



H57H-AD

V : 1.0

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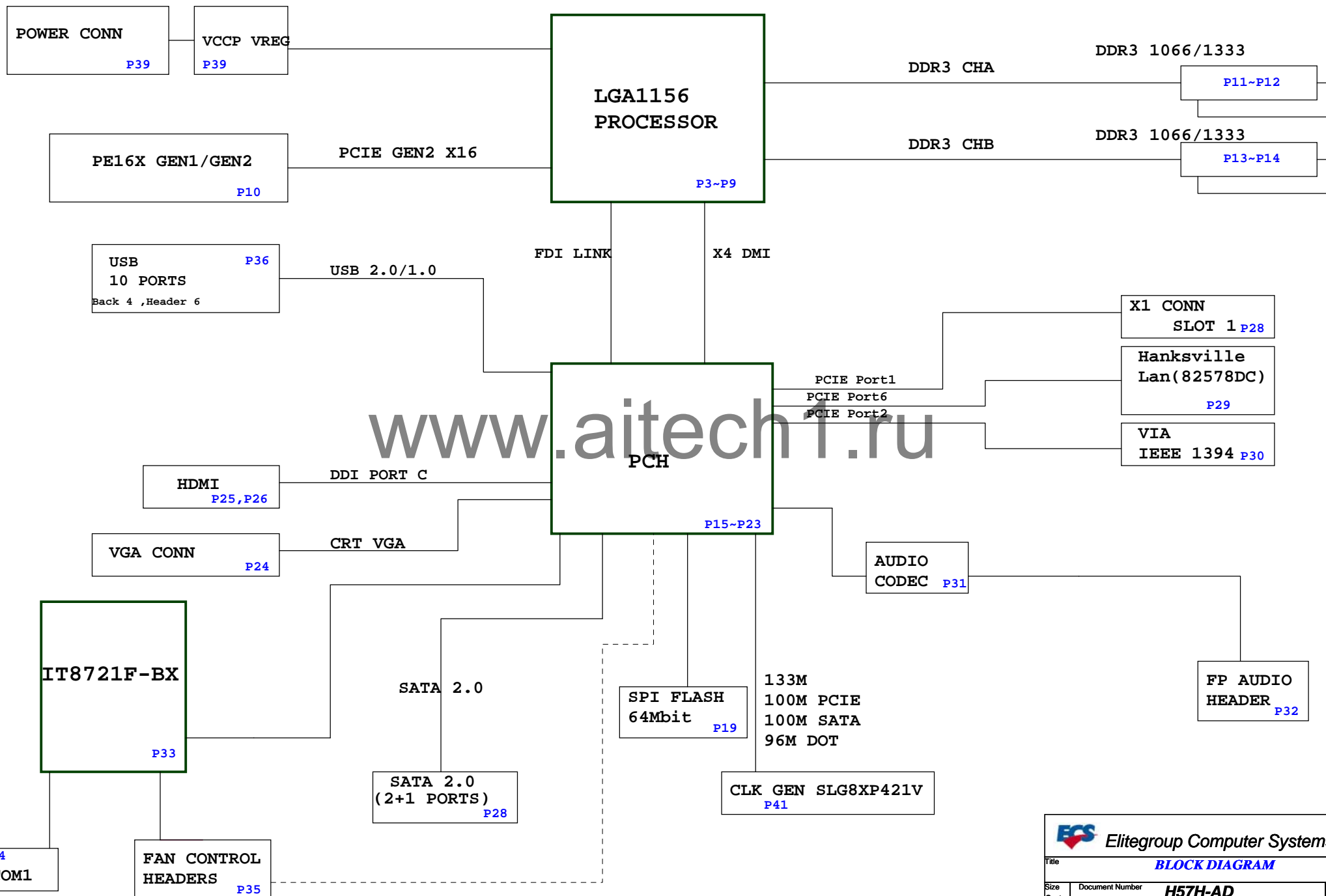
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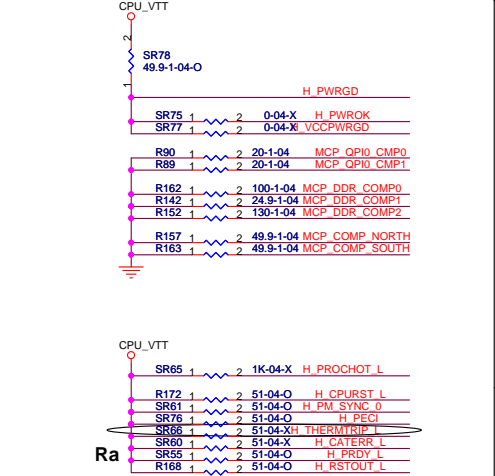
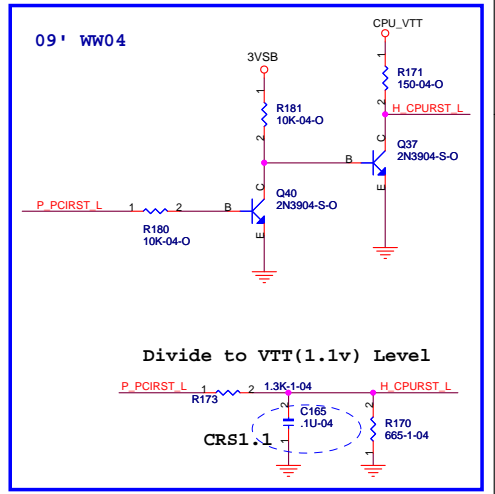
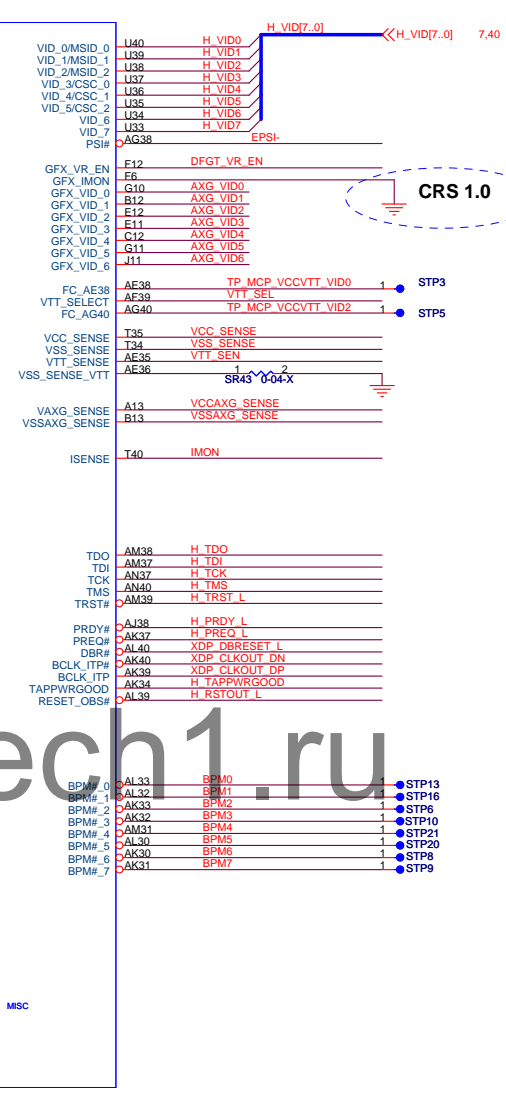
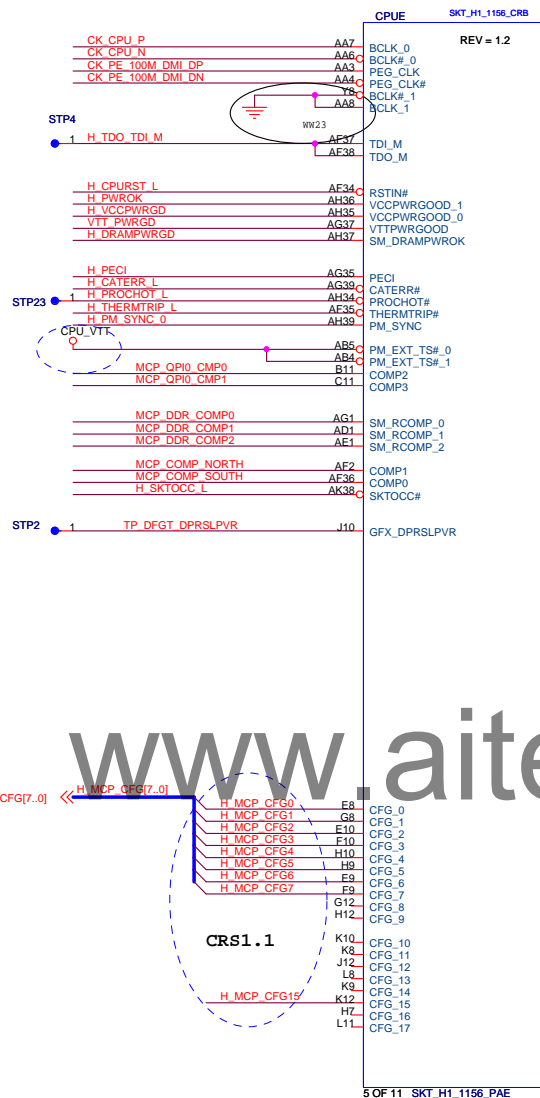
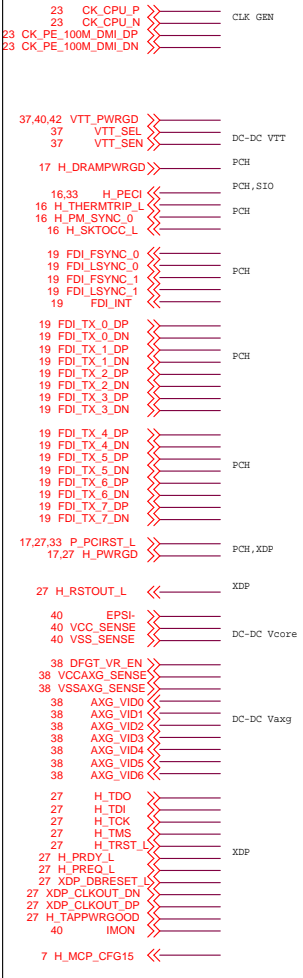
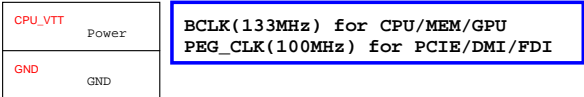
Rev	Date	Notes
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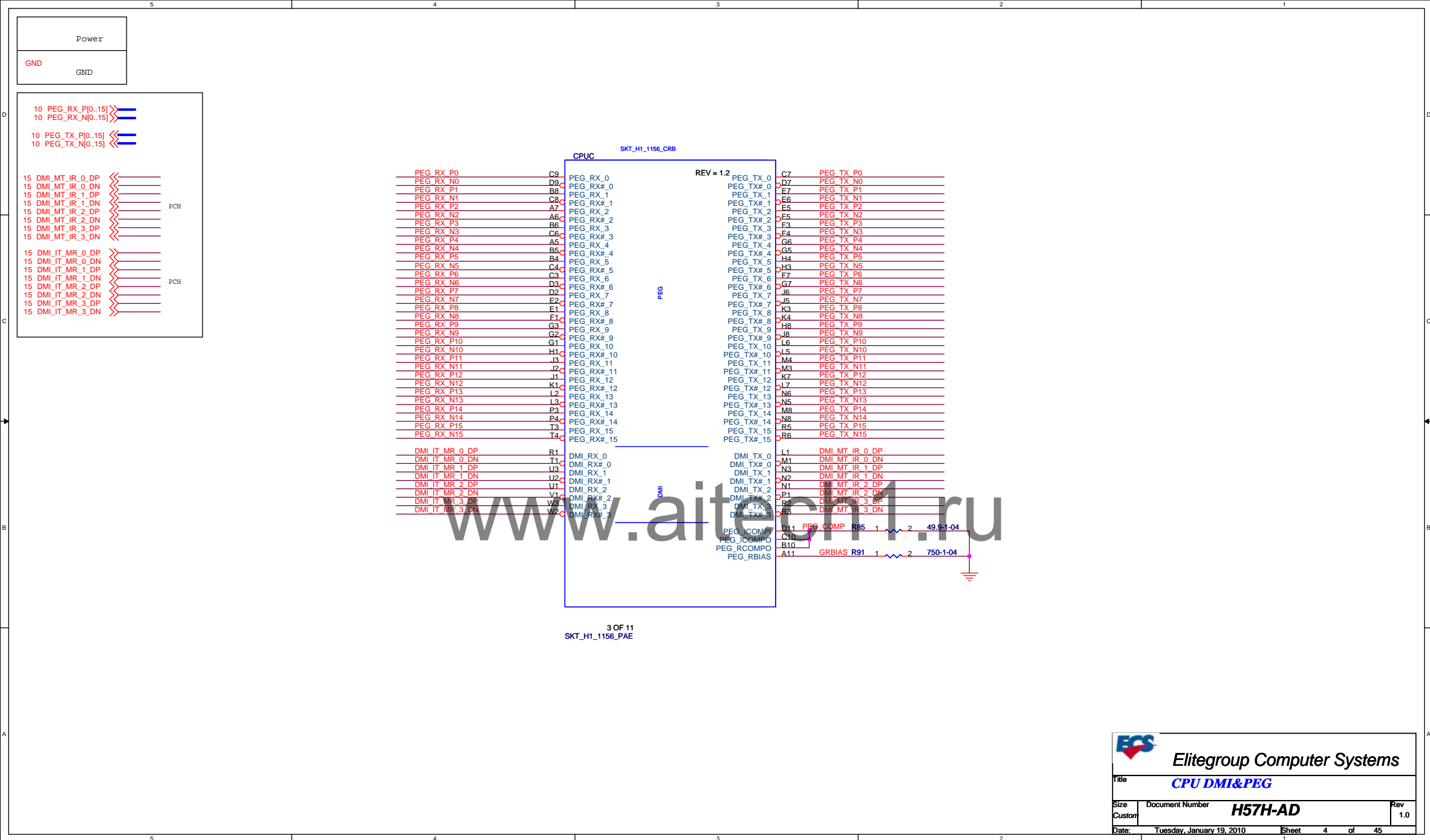
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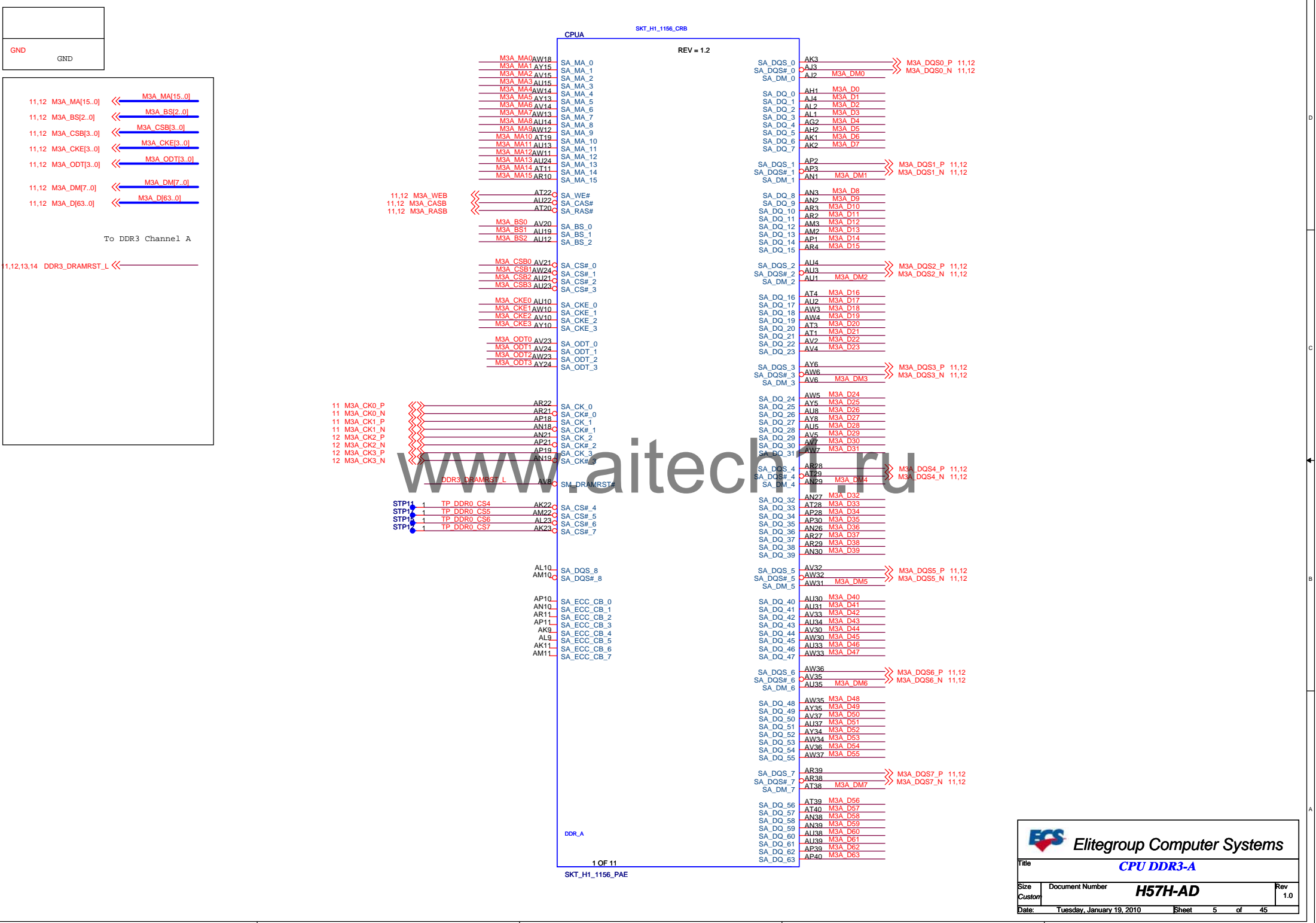
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Title <i>Cover Page</i>			
Size Custom	Document Number H57H-AD	Rev 1.0	
Date: Tuesday, January 19, 2010		Sheet 1	of 45

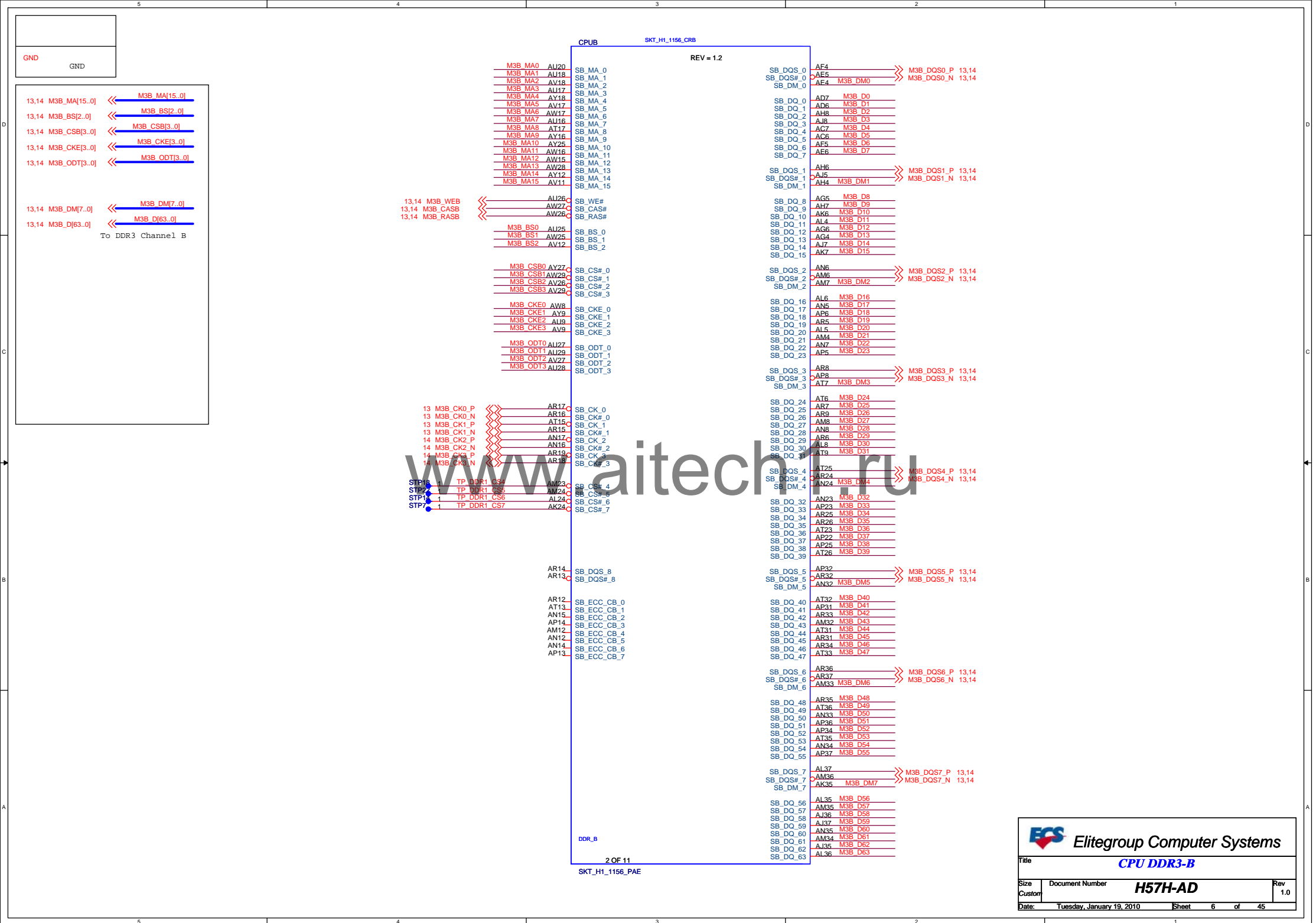




Ra for PRDY emptied

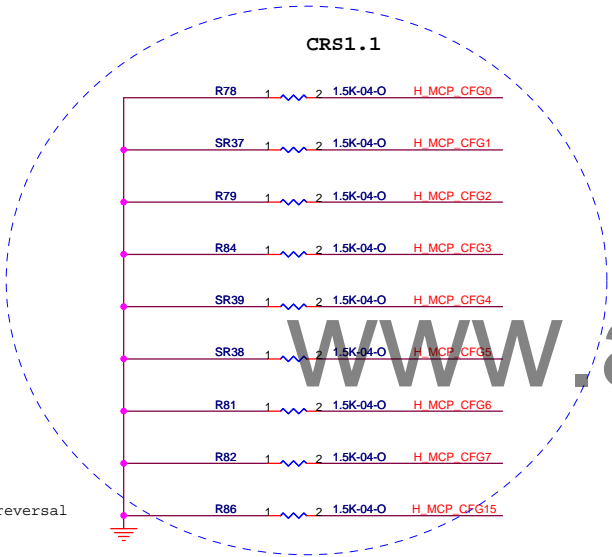






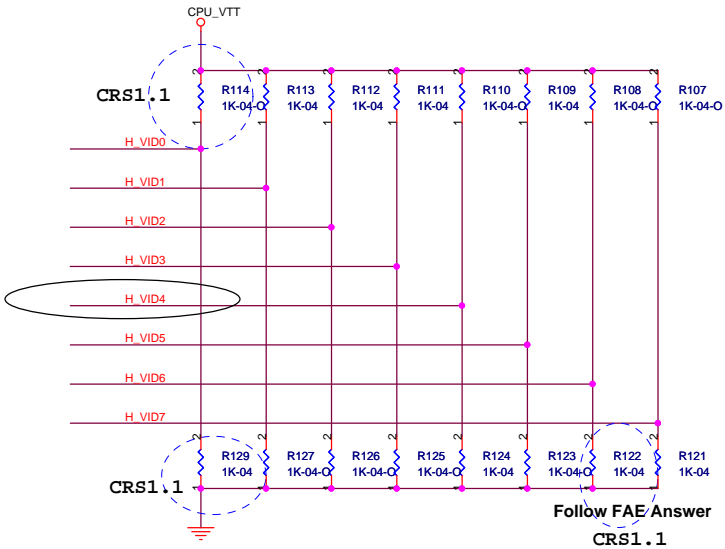
CPU_VTT	Power
GND	GND

3 H_MCP_CFG[7..0]	>> H_MCP_CFG[7..0]	CPU
3 H_MCP_CFG15	>> H_MCP_CFG15	
3.40 H_VID[7..0]	<< H_VID[7..0]	CPU, DC-DC Vcore



CFG(1:0)
 Desktop
 11 PCIE16X
 10 PCIE18X
 CFG2,4,5,6,7~17
 Reserved configuration land
 CFG3
 Havendale PCIE static Lan Numbering reversal

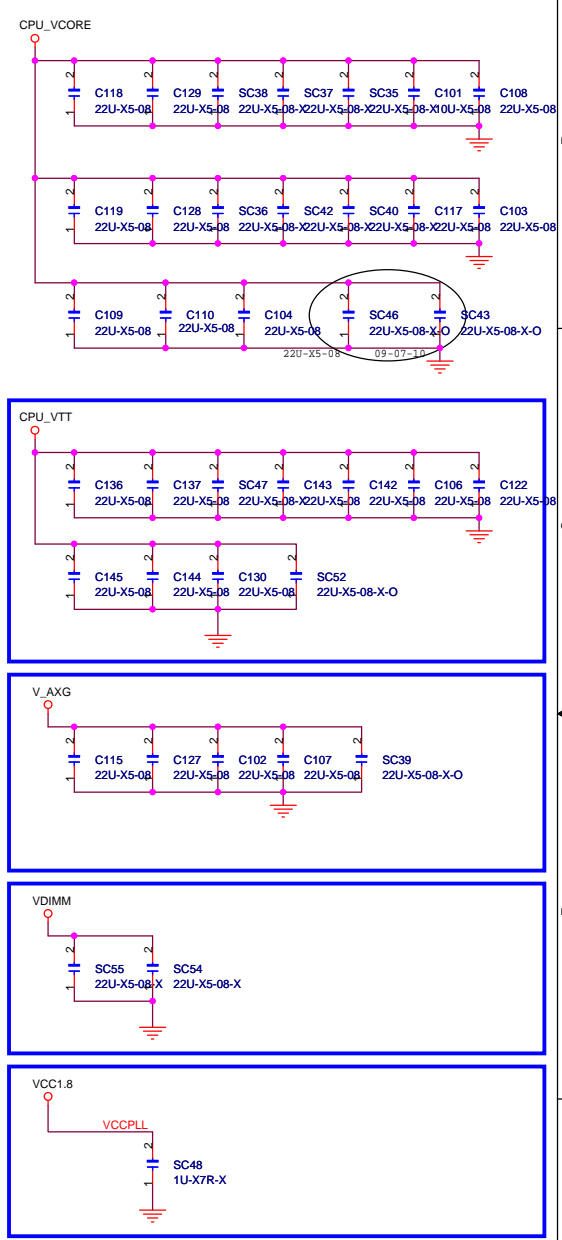
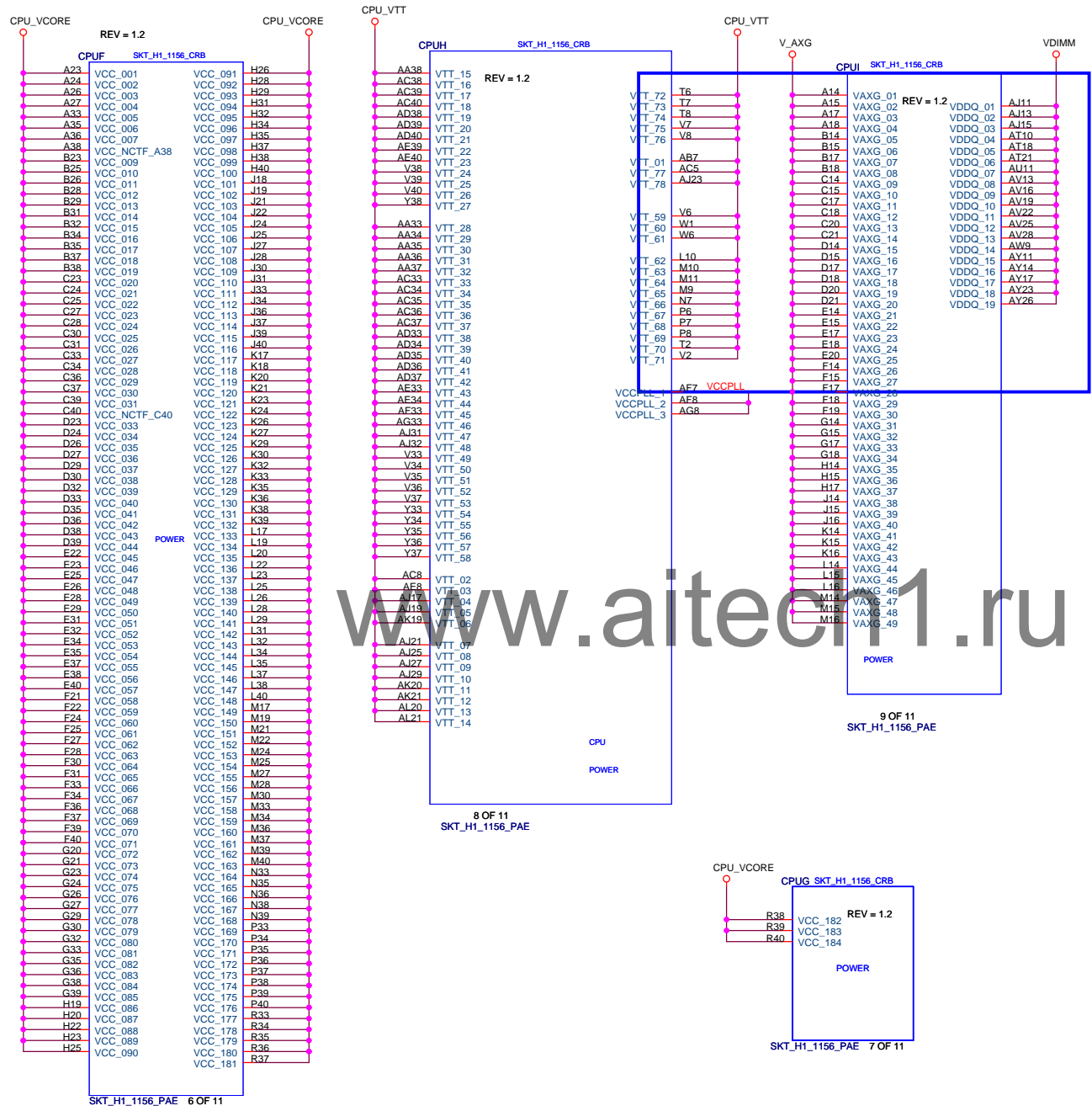
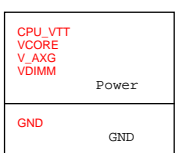
CFG	Havendale	Lynnfield			
0	REVERSED	1	11=1*16X	0	10=2*8X
1	REVERSED	1		1	
2	REVERSED			REVERSED	
3	Static Lane Number Reversal			REVERSED	
4	REVERSED			REVERSED	
6	REVERSED				
7	REVERSED				
15	REVERSED				
0,1,2,3,4,5 ALL HAVE INTERNAL PULL-UPS					

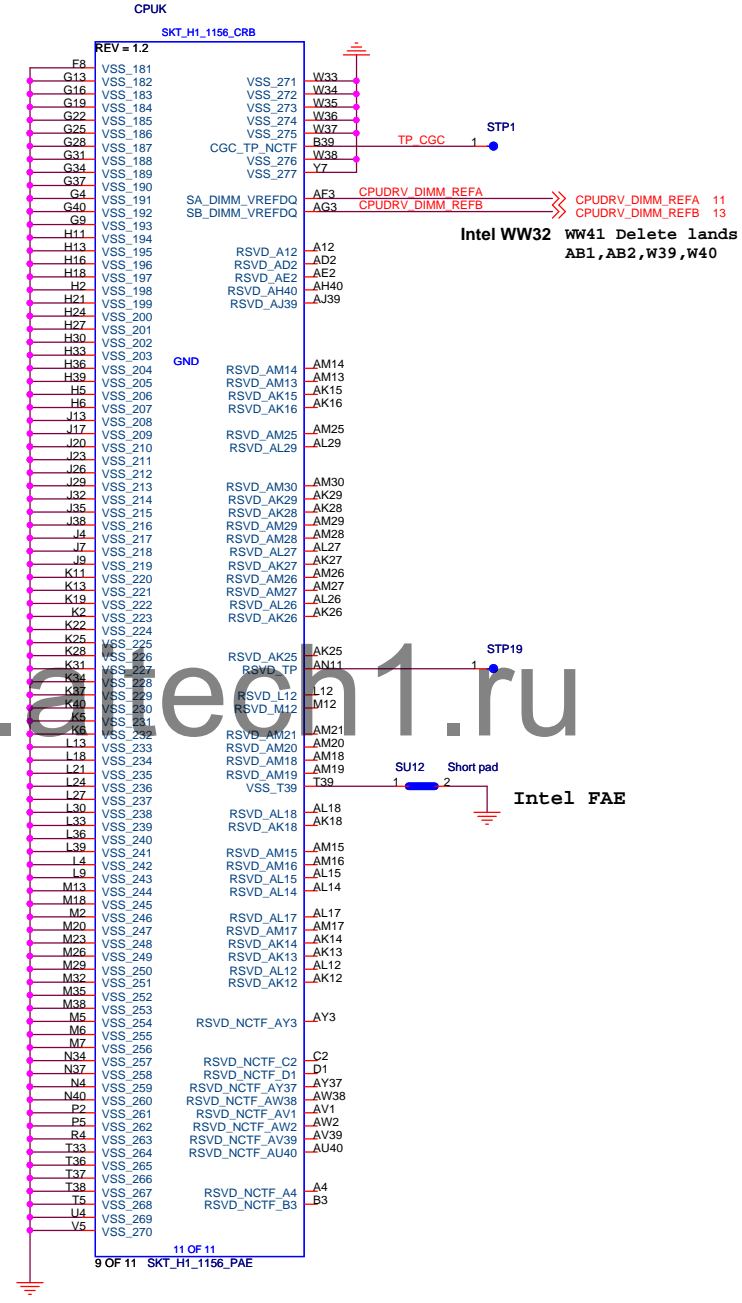
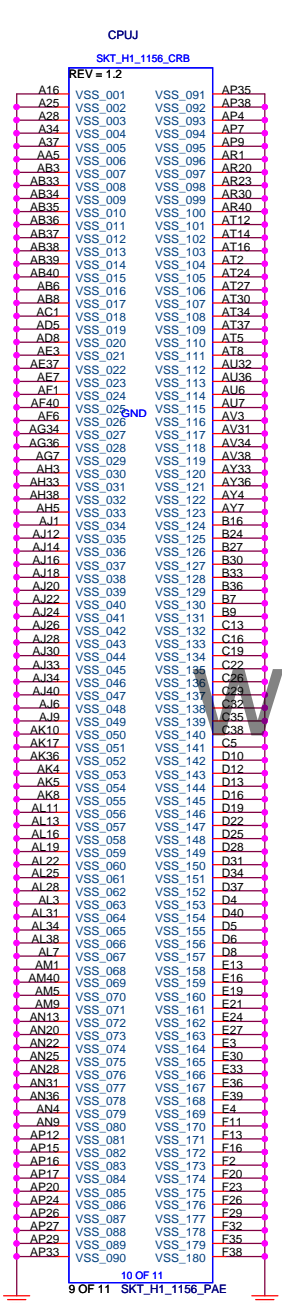
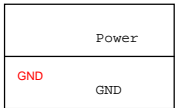


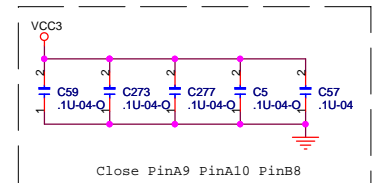
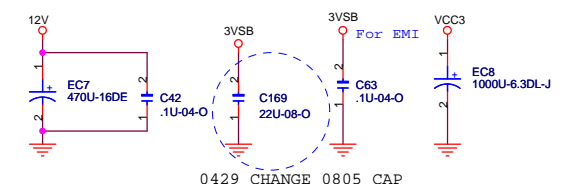
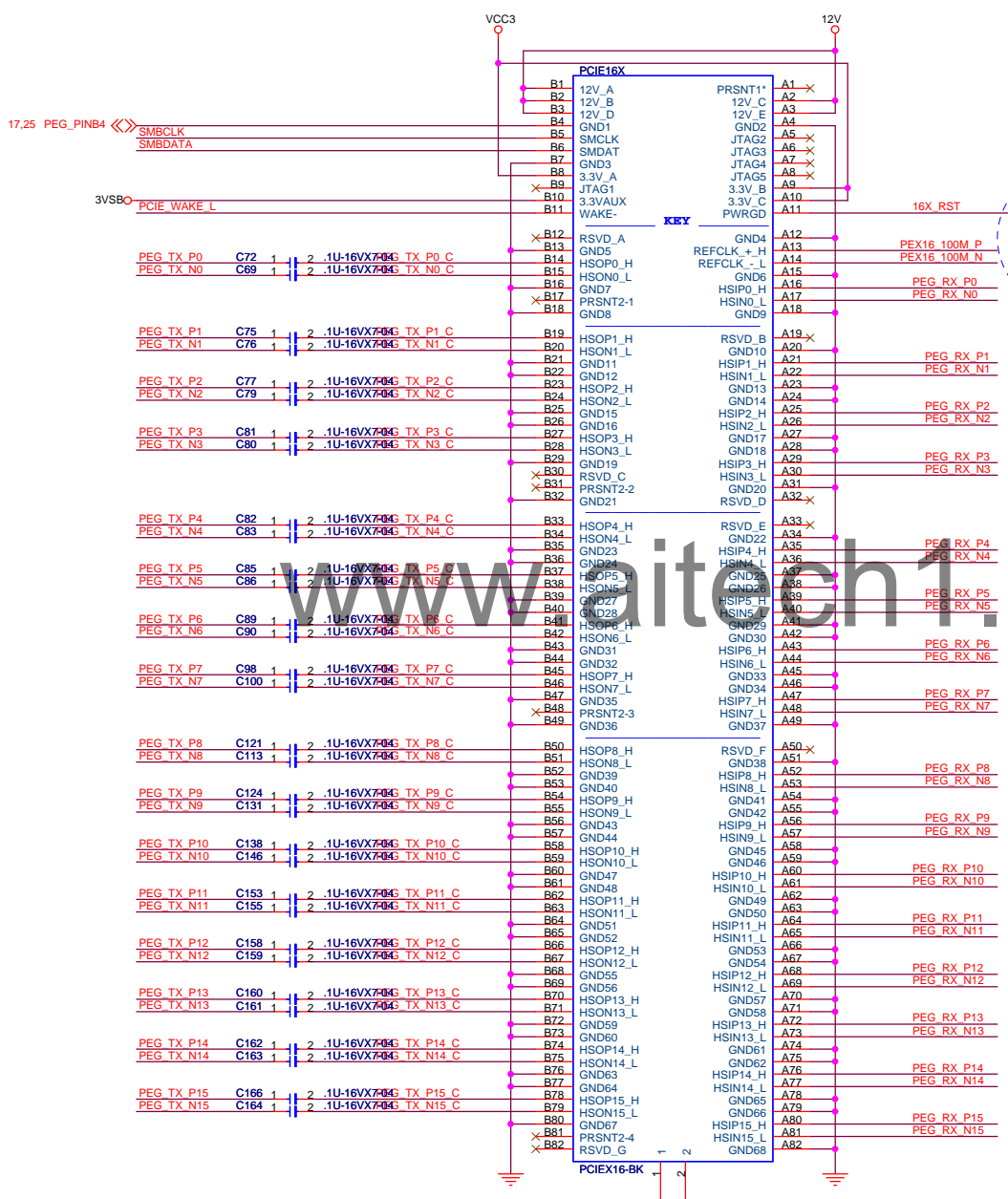
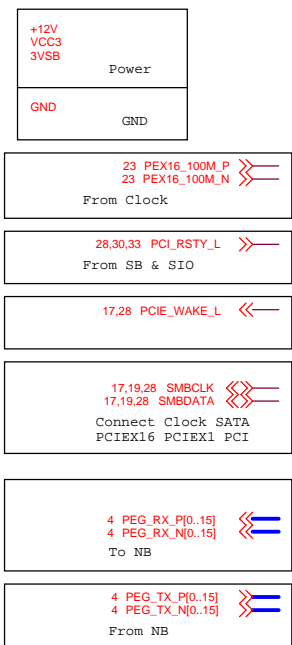
POWER ON CONFIGURATION (POC)TABLE

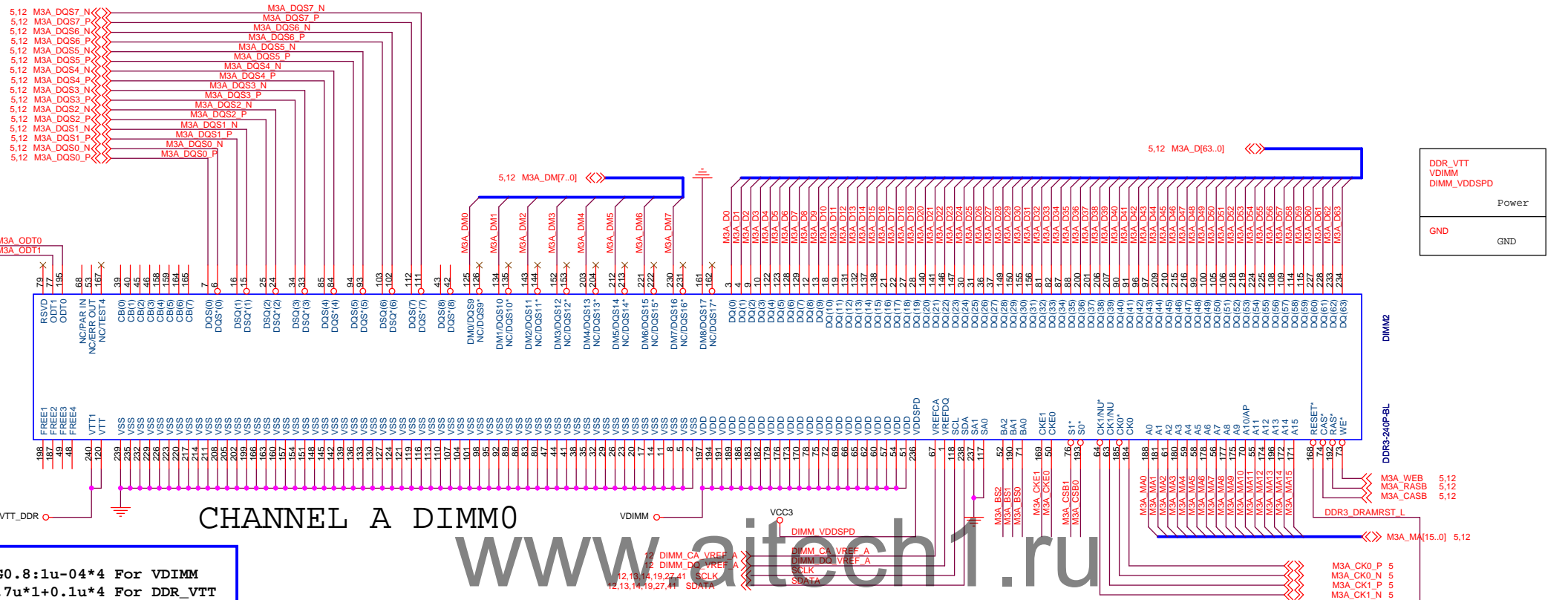
	FUNCTION	Setting	Havendale	Lynnfield
VID0	MIS0	0	Support	Support
VID1	MIS1	1		
VID2	MIS2	1	Icc(MAX)=120A	Icc(MAX)=120A
VID3	IMON CONFIG CSC0	1		
VID4	IMON CONFIG CSC1	0		
VID5	IMON CONFIG CSC2	1		
VID6	RESERVED	0		
VID7	VID SELECT	0		
PSI#	RESERVED	LOW		

*MSID(2:0)
 110 Lynnfield and Havendale support
 *CSC(0:2)
 Iout Gain and POC setting
 100 ICC(max) 80A~100A
 101 ICC(max) 100A~120A
 110 ICC(max) 120A~140A



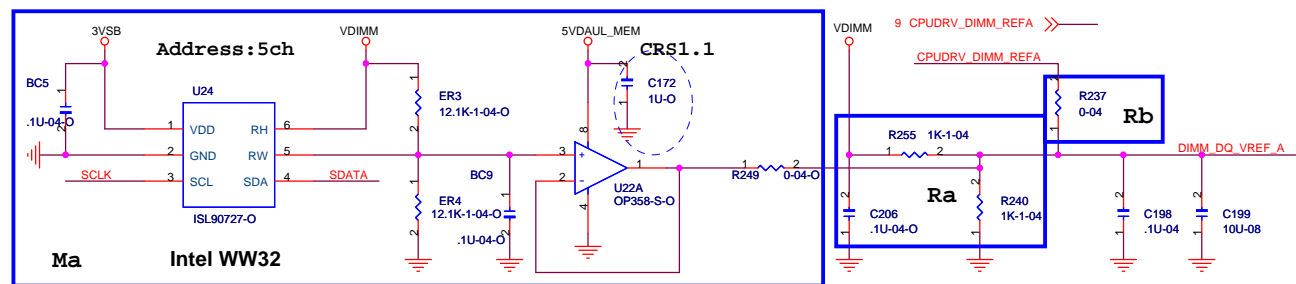
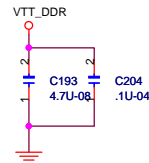
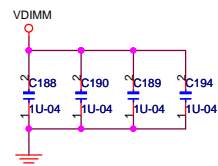




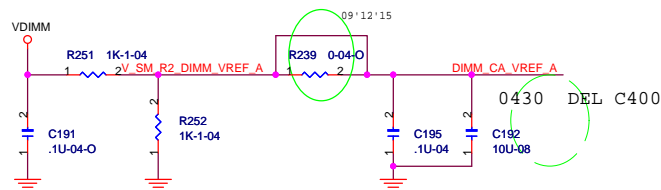


CHANNEL A DIMM0

DG0.8:1u-04*4 For VDIMM
4.7u*1+0.1u*4 For DDR_VTT
Per DIMM



DQ_VREF Control Mode	
Mode 1	Ra
Mode 2	Rb
Mode 3	Ma Ra=2.2OHM



6.13 M3B_DQS7_N
6.13 M3B_DQS7_P
6.13 M3B_DQS6_N
6.13 M3B_DQS6_P
6.13 M3B_DQS5_N
6.13 M3B_DQS5_P
6.13 M3B_DQS4_N
6.13 M3B_DQS4_P
6.13 M3B_DQS3_N
6.13 M3B_DQS3_P
6.13 M3B_DQS2_N
6.13 M3B_DQS2_P
6.13 M3B_DQS1_N
6.13 M3B_DQS1_P
6.13 M3B_DQS0_N
6.13 M3B_DQS0_P

M3B_ODT2
M3B_ODT3

6.13 M3B_DM[7..0]

6.13 M3B_D[63..0]

CHANNEL B DIMM1

13 DIMM_CA_VREF_B
13 DIMM_DQ_VREF_B
11,12,13,19,27,41 SCLK
11,12,13,19,27,41 SDATA

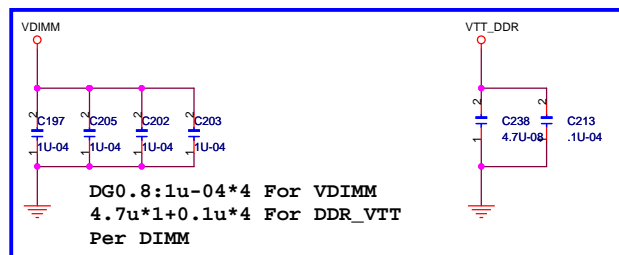
DIMM CA_VREF_B
DIMM DQ_VREF_B
SCLK
SDATA

M3B_CK2_P 6
M3B_CK2_N 6
M3B_CK3_P 6
M3B_CK3_N 6

DDR3_DRAMRST_L 5,11,12,13

DDR3-240P-GR
M3B_WEB 6,13
M3B_RASB 6,13
M3B_CASB 6,13

DIMM3



6.13 M3B_MA[15..0]

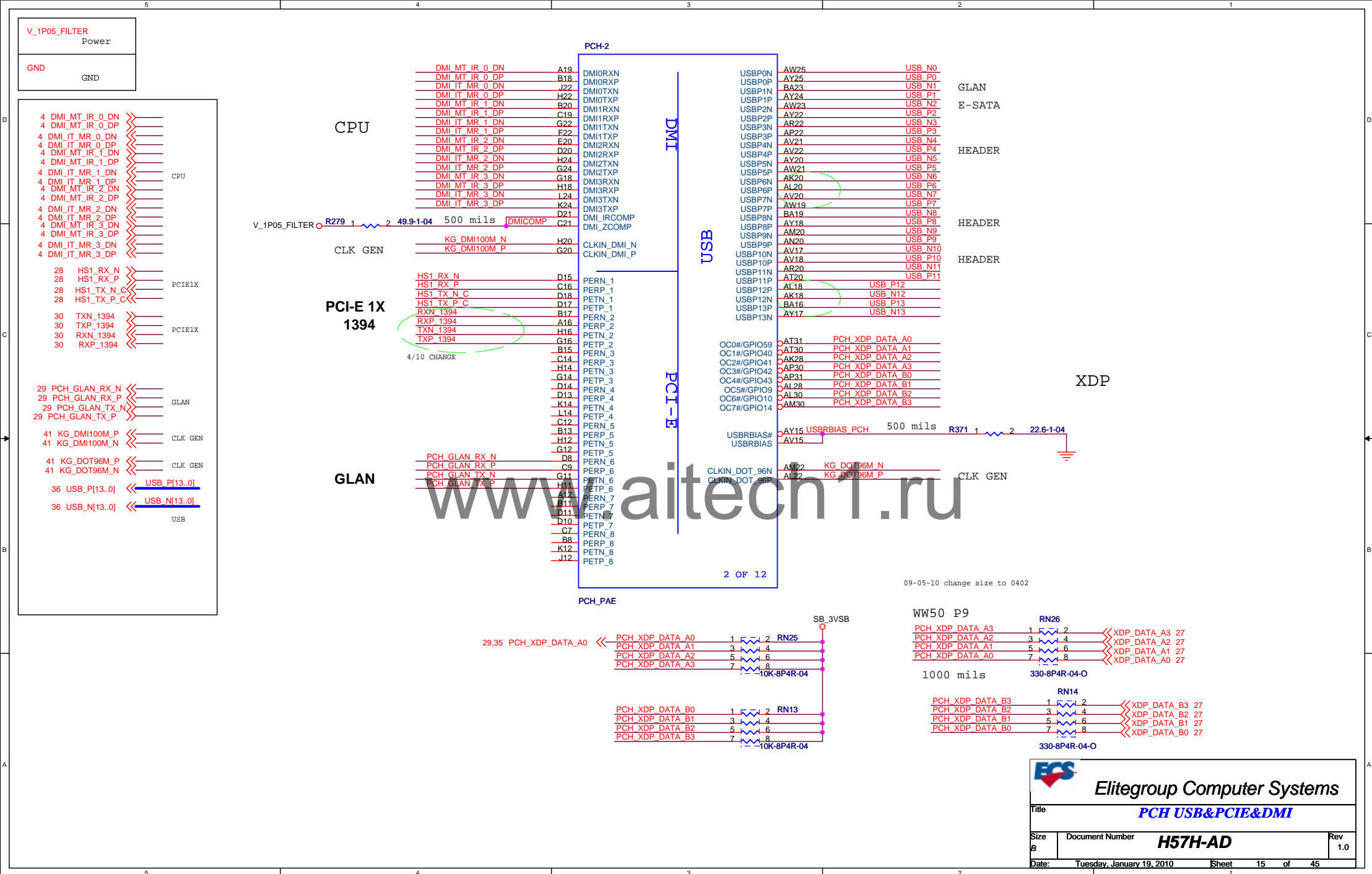
6.13 M3B_ODT3[3..0]

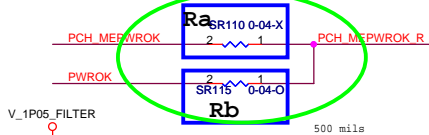
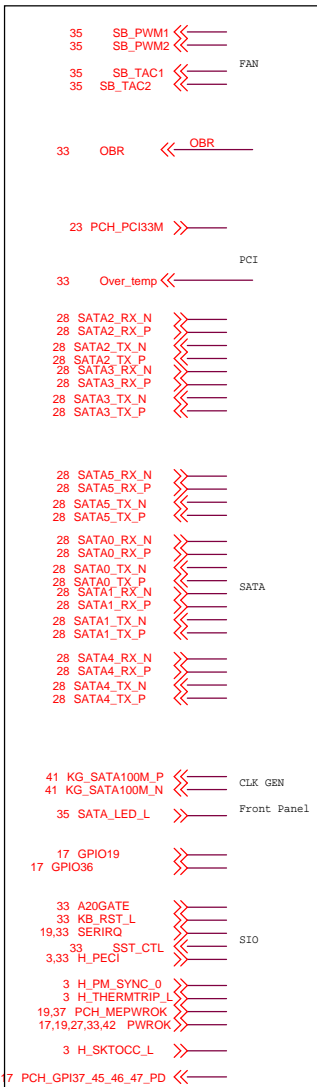
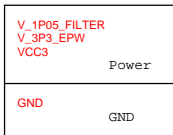
6.13 M3B_CSB[3..0]

6.13 M3B_CKE[3..0]

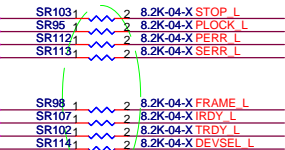
6.13 M3B_BS[2..0]

DDR_VTT	Power
VDIMM	
DIMM_VDDSPD	
GND	GND





ME_PWROK		
AMT		Ra
Non-AMT		Rb



0421 change RN TO R

H_SKT0CC_L R367 1 2 0-04-O XDP_GP28 >>> XDP_GP28 17,27

DESIGN NOTE: BIOS
Al6 Swap override
Override if sampled low

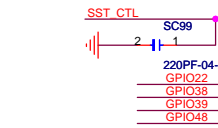
DESIGN NOTE: Server Only
DMI AC COUPLING
FULL VOLTAGE MODE WHEN SAMPLED LOW
Desktop Platform do't pull low

BOOT DEVICE	GNT1	GNT0
LPC	0	0
PCI	1	0
SPI	1	1

WW 11 PCI CHANGE TO 10

FAN

NOT USE

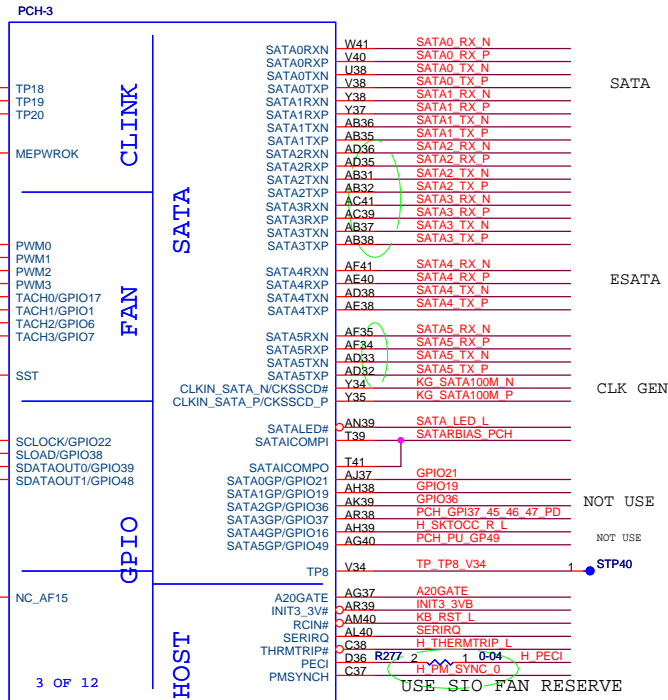


0504 del PAR-PME-PCIRST



PULL UP

PULL UP



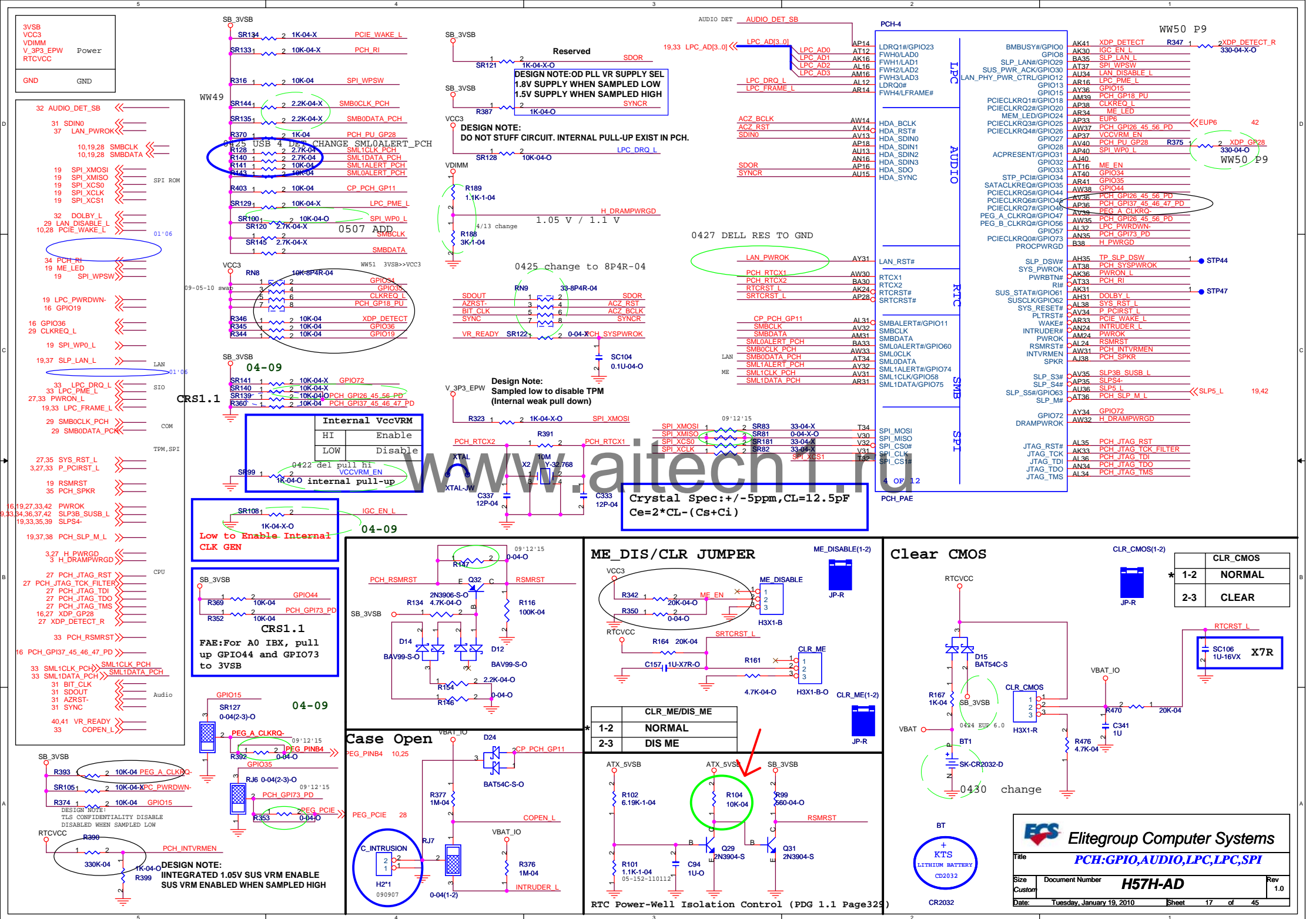
SATA

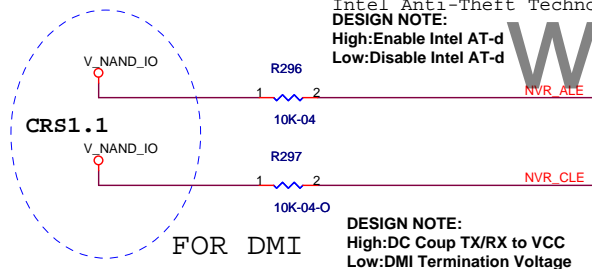
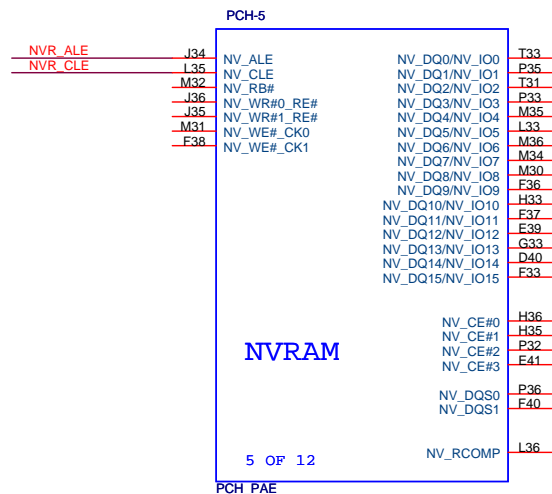
ESATA

CLK GEN

NOT USE

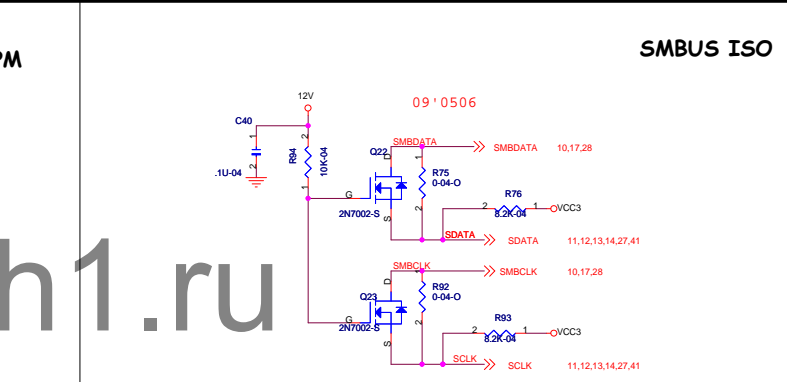
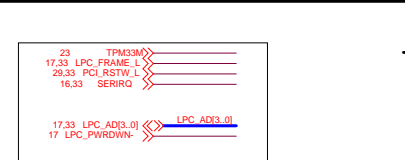
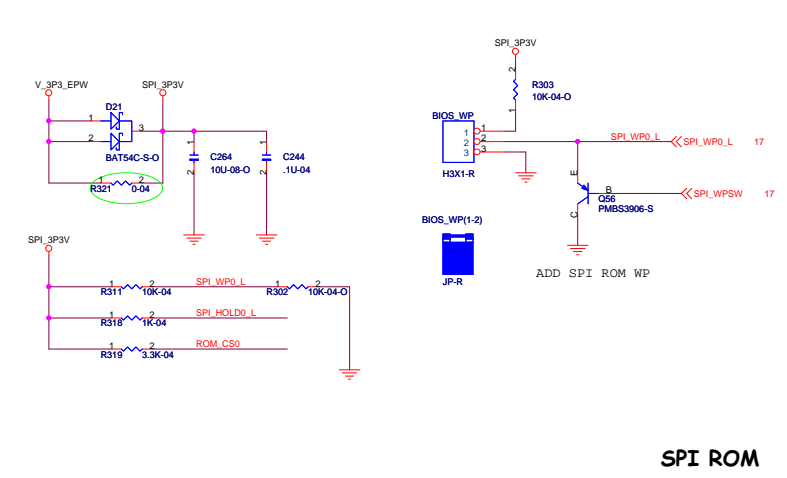
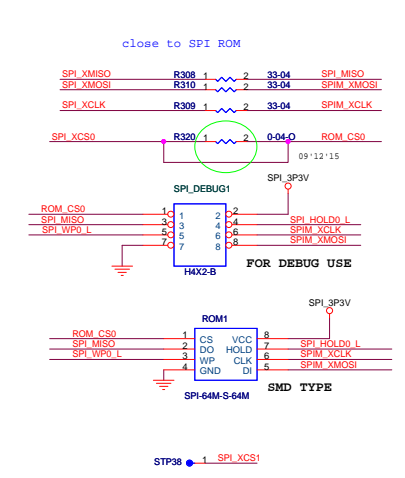
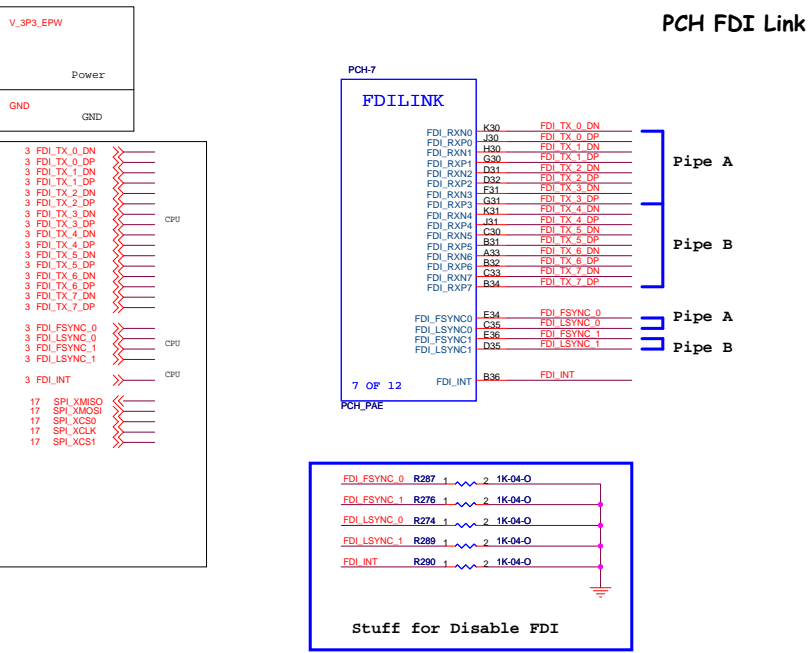
NOT USE

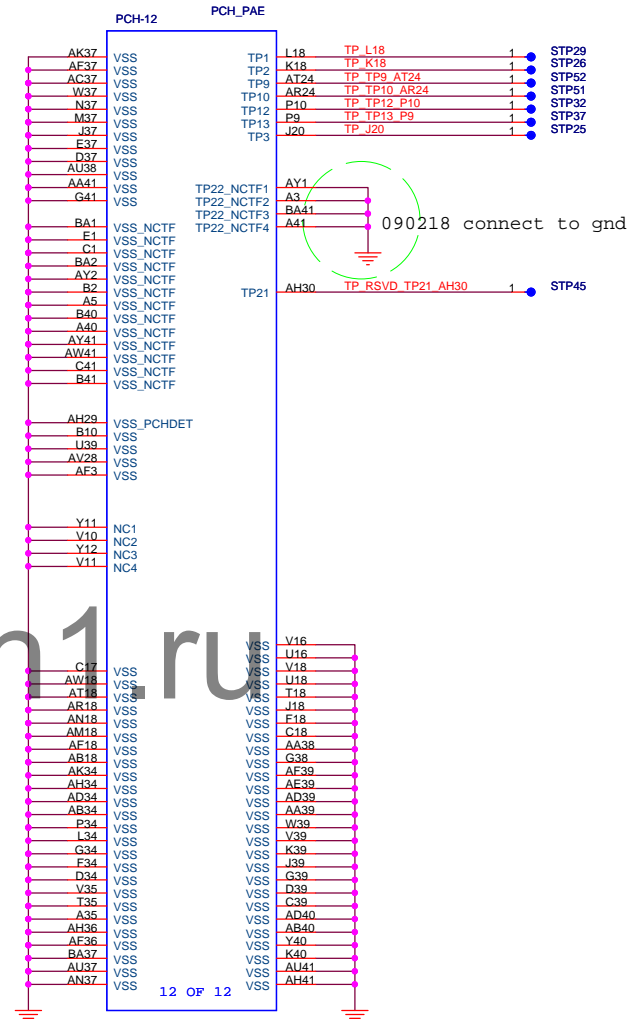
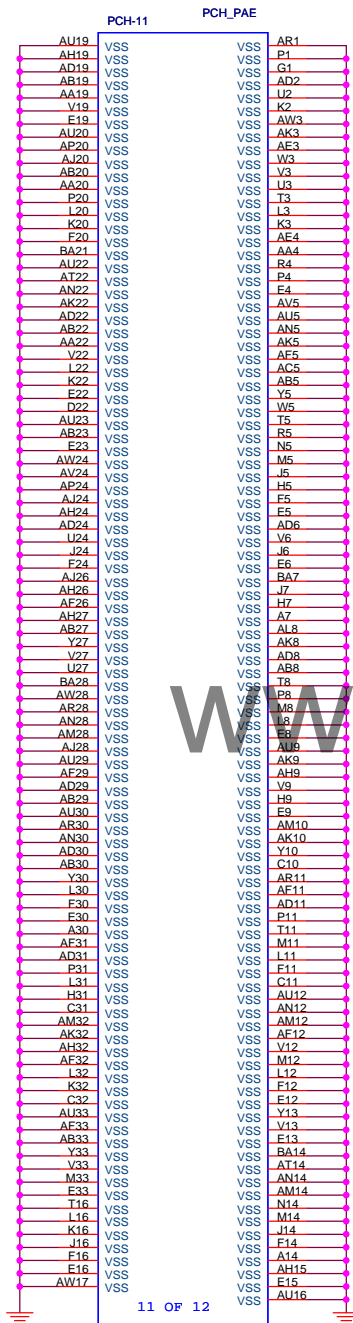


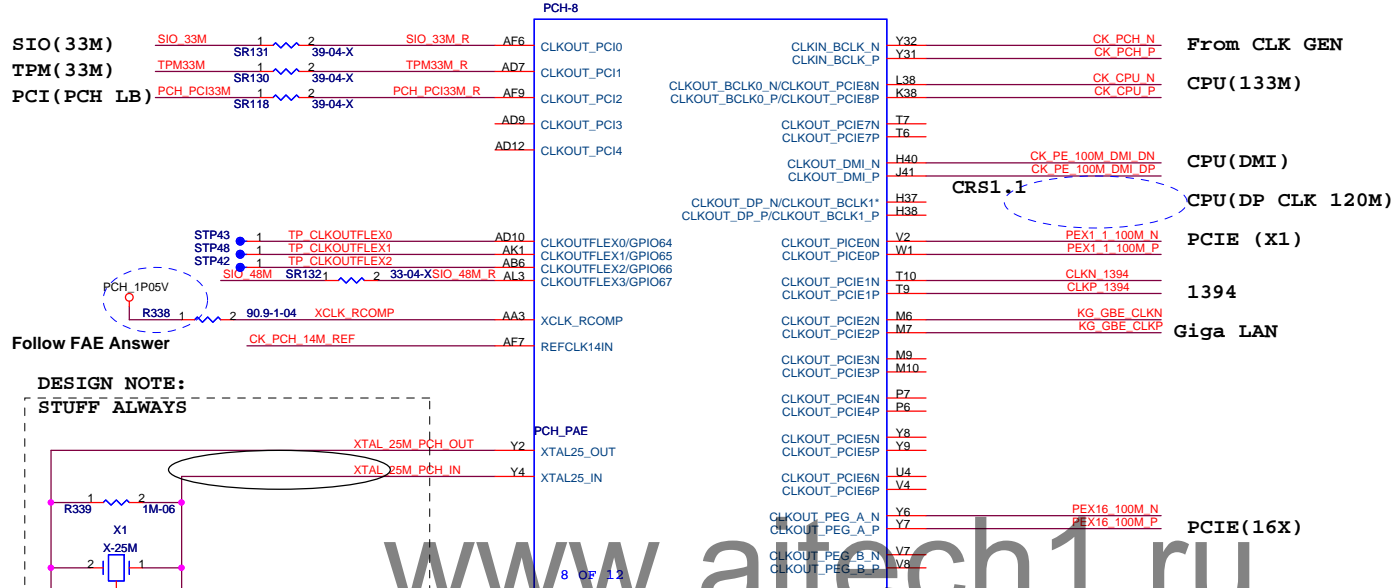
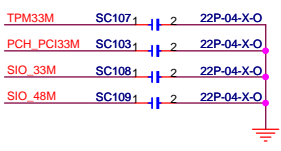
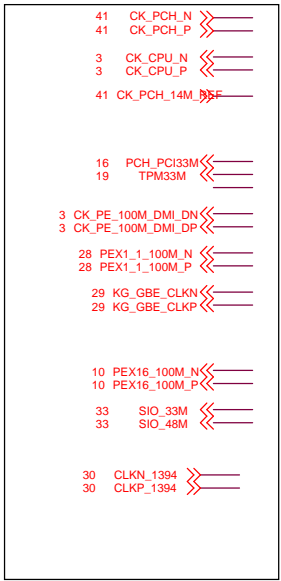


DESIGN NOTE:
High:Enable Intel AT-d
Low:Disable Intel AT-d

DESIGN NOTE:
High:DC Coup TX/RX to VCC
Low:DMI Termination Voltage

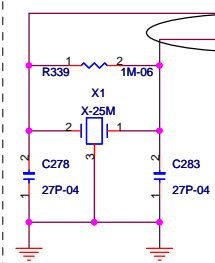






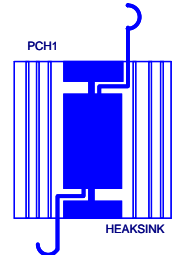
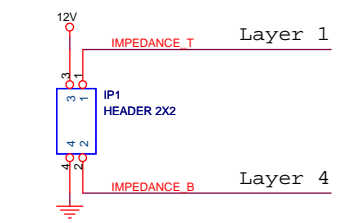
Follow FAE Answer

DESIGN NOTE:
STUFF ALWAYS



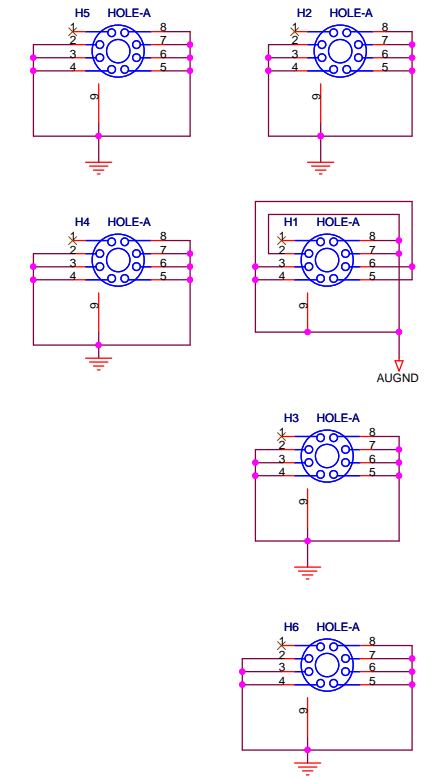
DESIGN NOTE:
R128 DAMPING RESISTOR
DO NOT CHANGE TO 0402

Crystal Spec: +/- 30ppm, CL=20pF
Ce=2*CL (Cs+Ci)

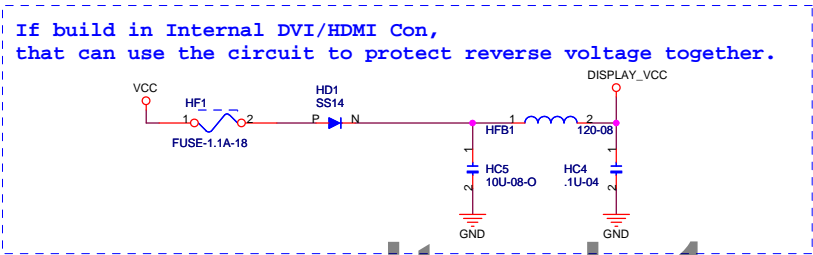
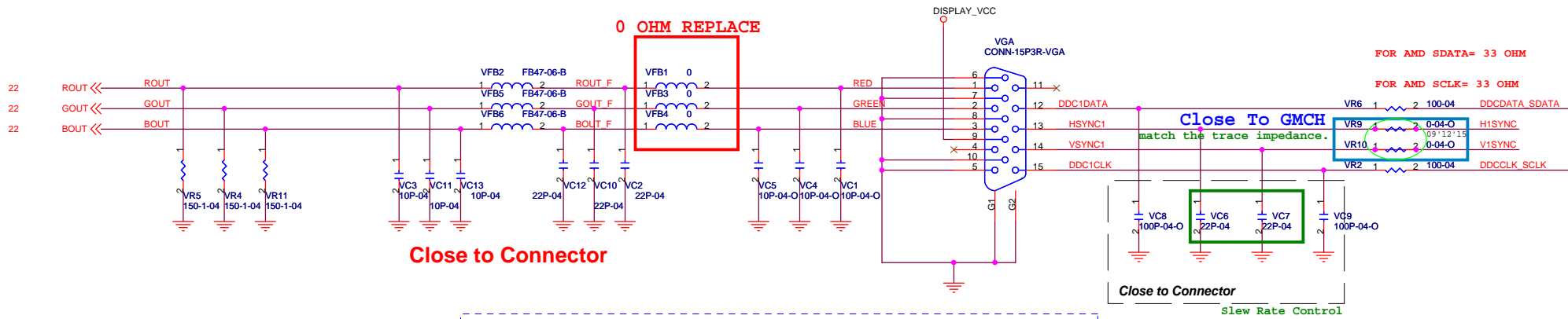


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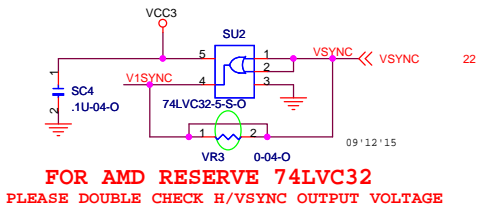
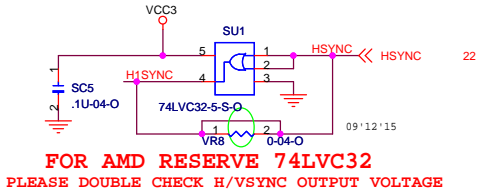
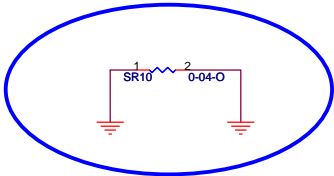
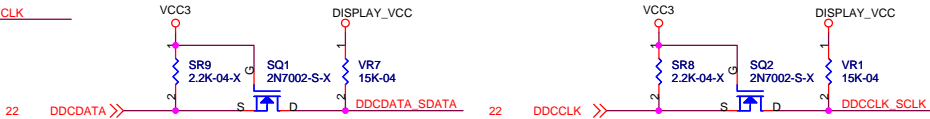
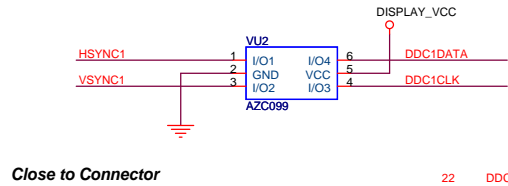
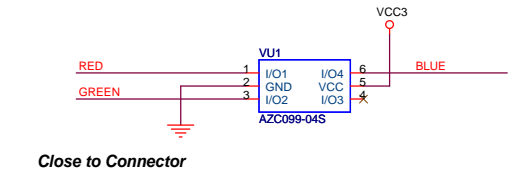
1080 : trace width 4 mil 50 ohm
Trace Length 3150 mils
Spacing: 1.clearance to itself 50/4/50(S:W:S)
2.clearance to other signal 3W

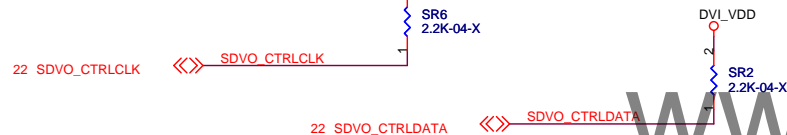
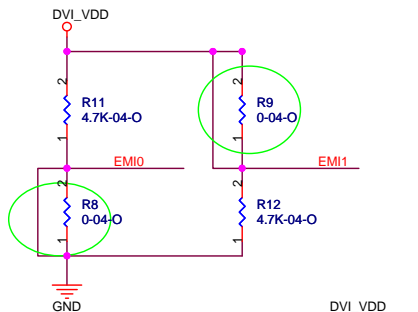
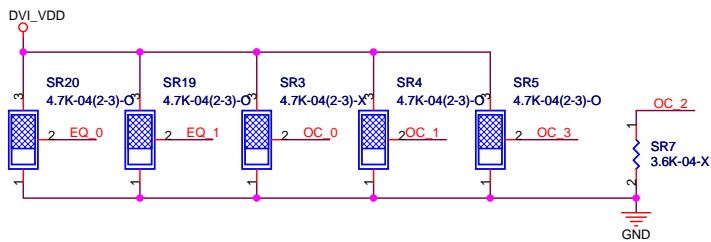


VGA Connector

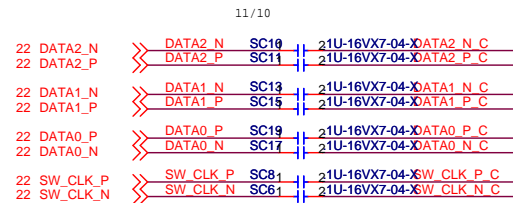


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	PS8101	PI3VDP411LSTZDES
EQ_0	RESERVE 4.7K PULL UP	RESERVE 4.7K PULL DOWN
EQ_1	RESERVE 4.7K PULL UP	RESERVE 4.7K PULL DOWN
OC_0	4.7K PULL UP	RESERVE 4.7K PULL DOWN
OC_1	RESERVE 4.7K PULL UP	RESERVE 4.7K PULL DOWN
OC_2	499 1% OHM PULL DOWN	RESERVE 4.7K PULL DOWN
OC_3	NC	RESERVE 4.7K PULL DOWN
PEG_PINB4	RESERVE 4.7K PULL UP	NC
HR20	NC	20K-04



DDC_EN	Passgate
3.3V	Enable
0	Disable

22 HPD >> 3.3V level

10,17 PEG_PINB4 >>

OC_3 >> 10

OC_0 >> 3

OC_1 >> 4

OC_2 >> 6

EQ_0 >> 34

EQ_1 >> 35

EQ_0 >> 34

EQ_1 >> 35

EQ_0 >> 34

EQ_1 >> 35

EQ_0 >> 34

EQ_1 >> 35

EQ_0 >> 34

EQ_1 >> 35

EQ_0 >> 34

EQ_1 >> 35

EQ_0 >> 34

EQ_1 >> 35

EQ_0 >> 34

EQ_1 >> 35

EQ_0 >> 34

EQ_1 >> 35

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EQ_0 >> 34

EQ_1 >> 35

EQ_0 >> 34

EQ_1 >> 35

EQ_0 >> 34

EQ_1 >> 35

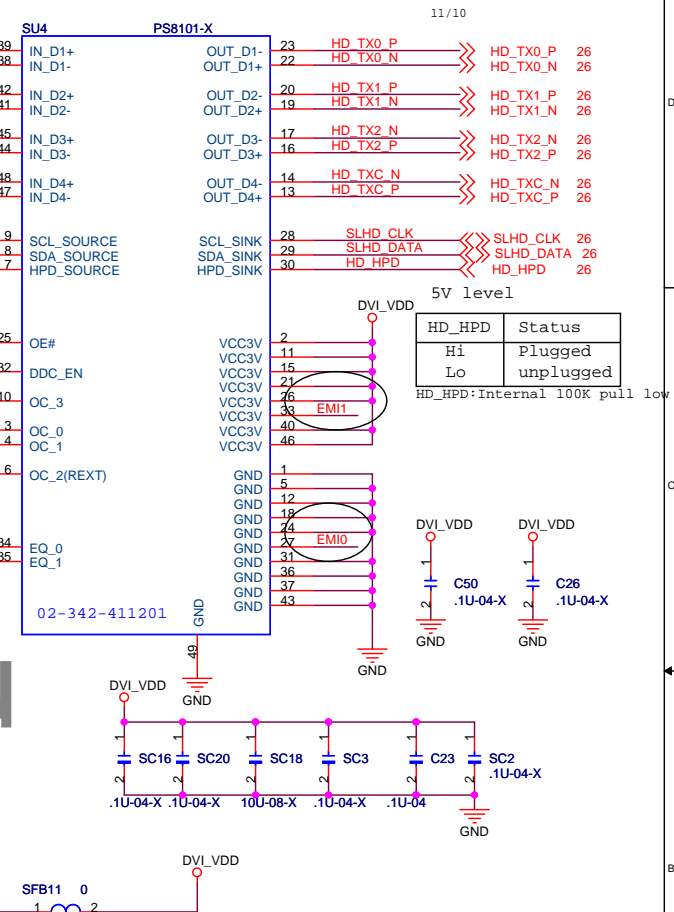
EQ_0 >> 34

EQ_1 >> 35

EQ_0 >> 34

EQ_1 >> 35

Level Shifter



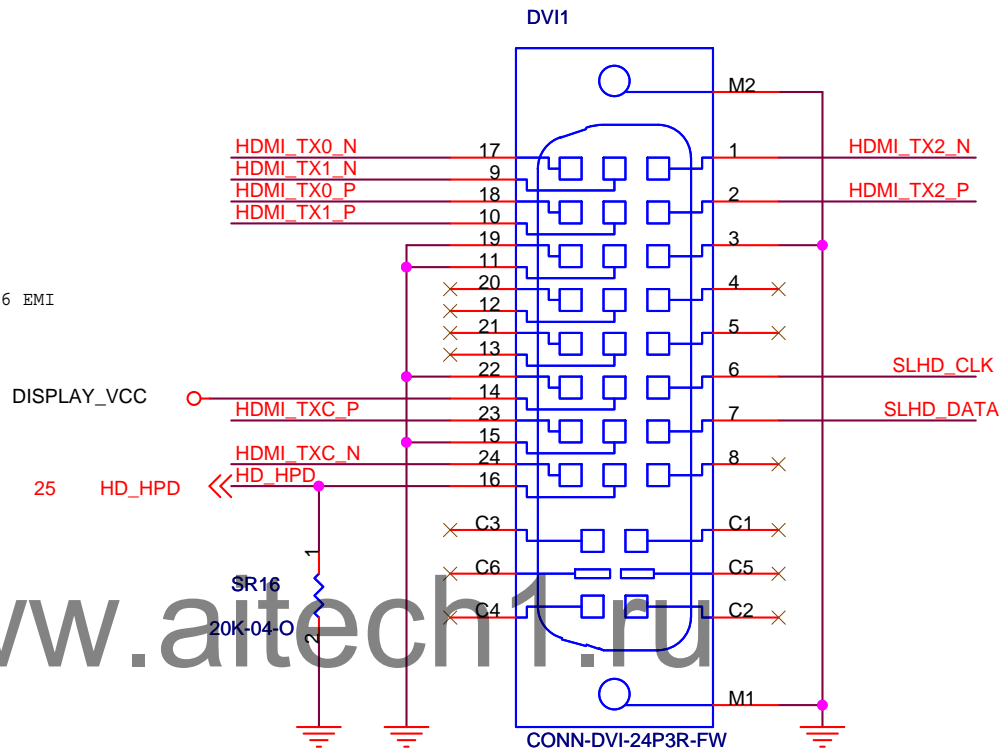
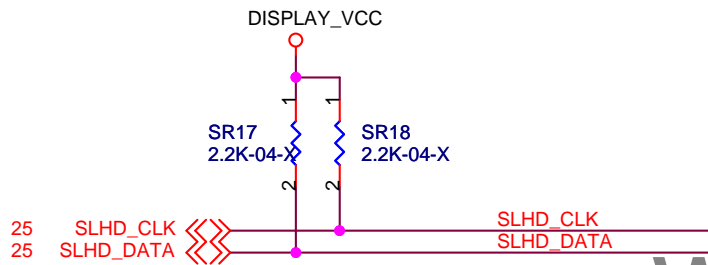
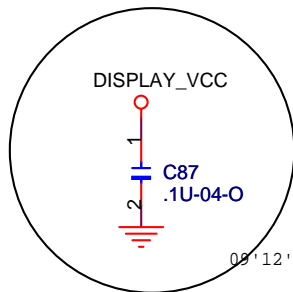
FOR PS8101			FOR PI3VDP411LSTZDES		
OC_3	OC_2	OC_1	OC_0	Vswing(mV)	Pre/De-emphasis
0	0	0	0	500	0
0	0	0	1	600	0
0	0	1	0	750	0
1	1	1	1		

EQ_0	EQ_1	Equalization(dB)
0	0	3
0	1	7.2
1	0	10
1	1	20

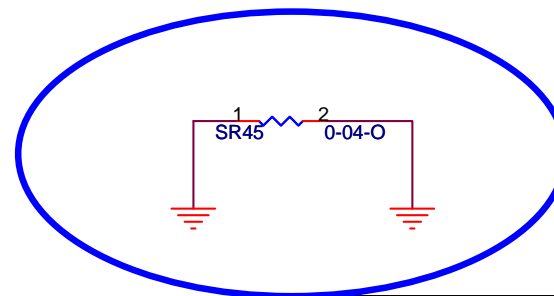
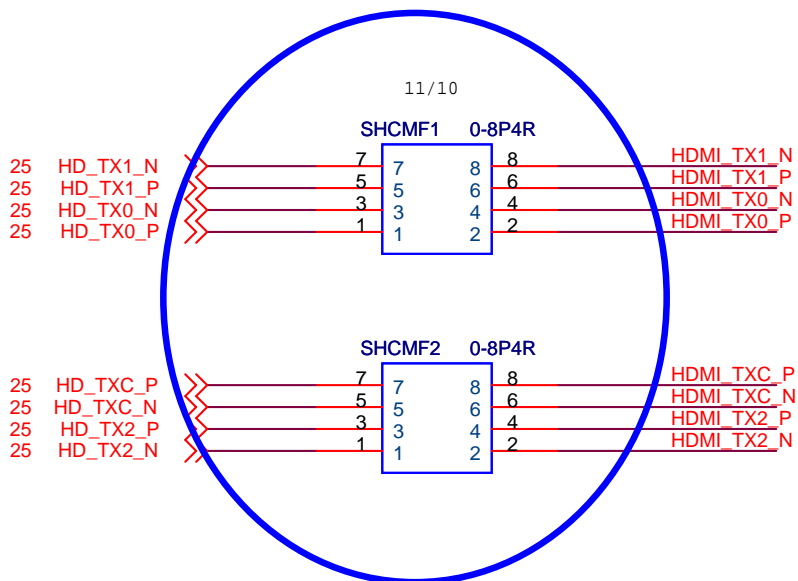


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Title		HDMI Interface (Switch, Level shifter)	
Size	Document Number	H57H-AD	
Custom			
Date:	Tuesday, January 19, 2010	Sheet	25 of 45



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CO-Lay COMMON CHOKE 8P4R

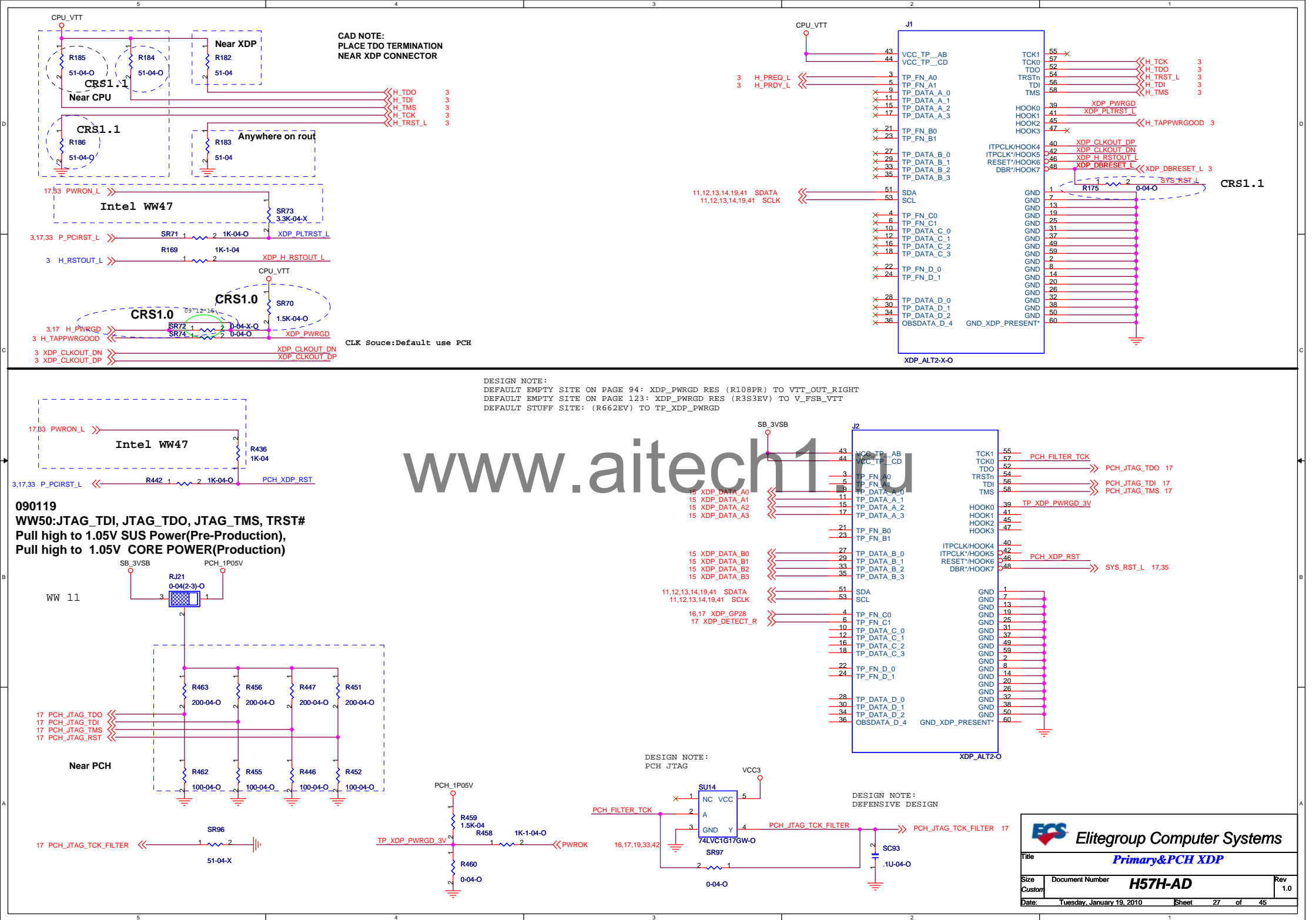
Elitegroup Computer Systems

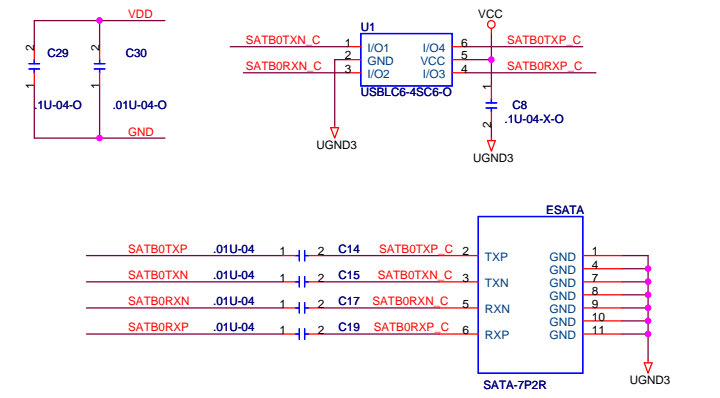
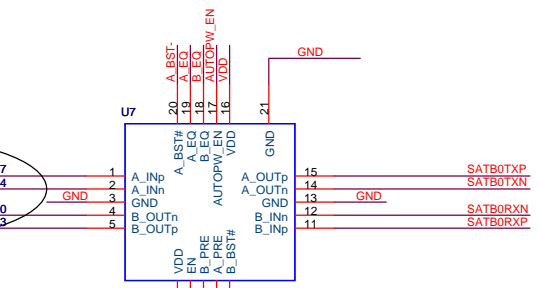
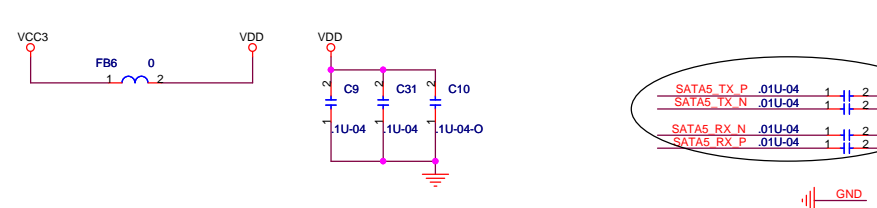
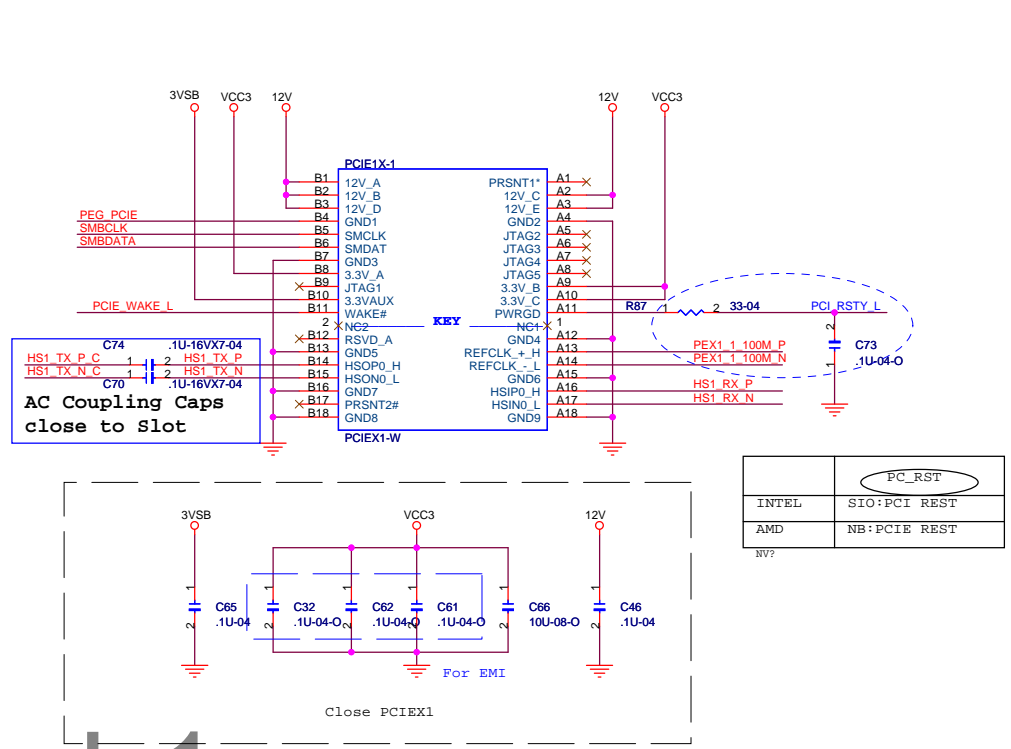
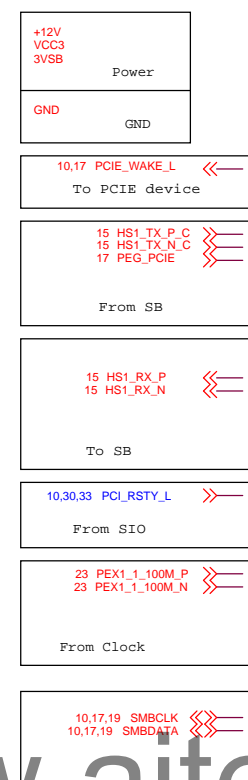
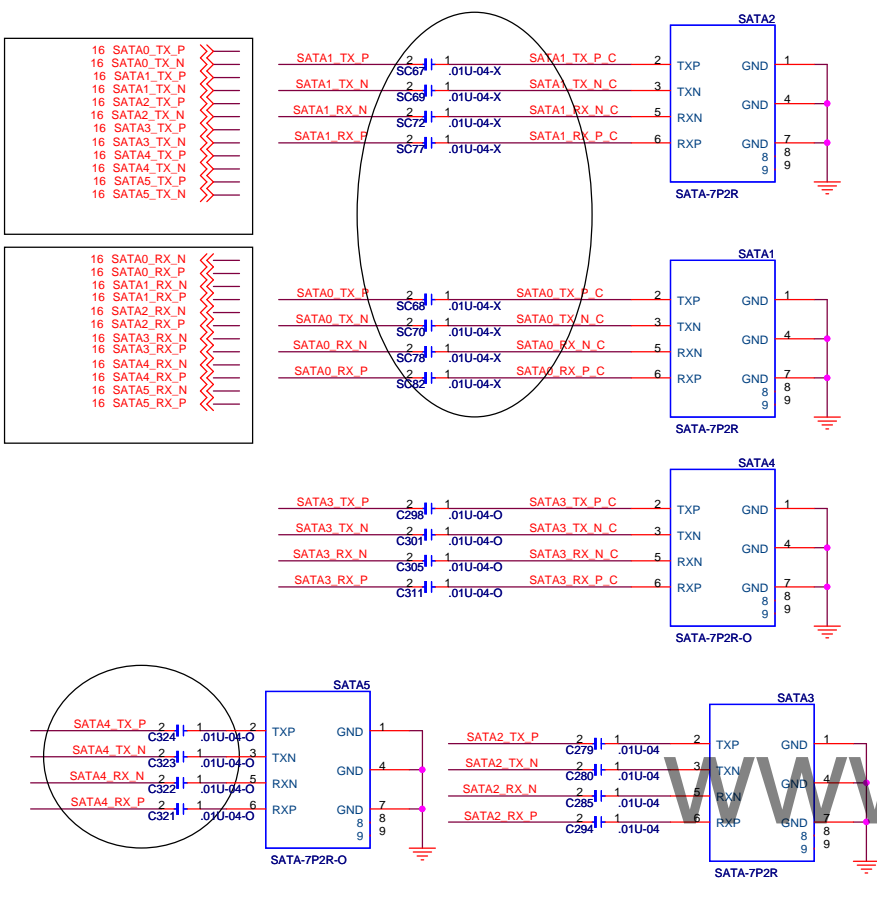
Title **HDMI CONN**

Size A Document Number **H57H-AD**

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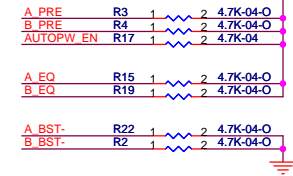


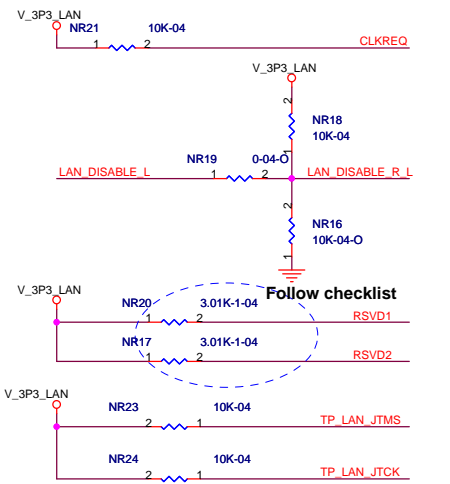
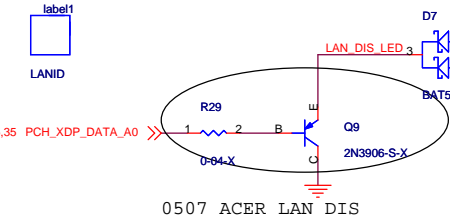
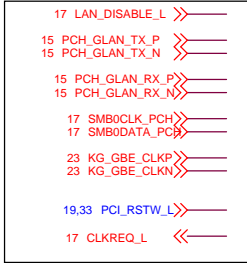
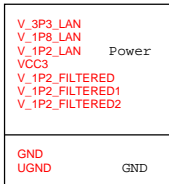
Output Level Boost setting: Internal pull up ~150Kohm
A_BST#B_BST# = HIGH, SATAi/m output level 400~700mVpp
A_BST#B_BST# = LOW, SATAx output level 800~1200mVpp

Automatic Power Saving Enable: Internal pull down ~150Kohm
AUTOPW_EN = HIGH, automatic power saving enable
AUTOPW_EN = LOW, automatic power saving disable

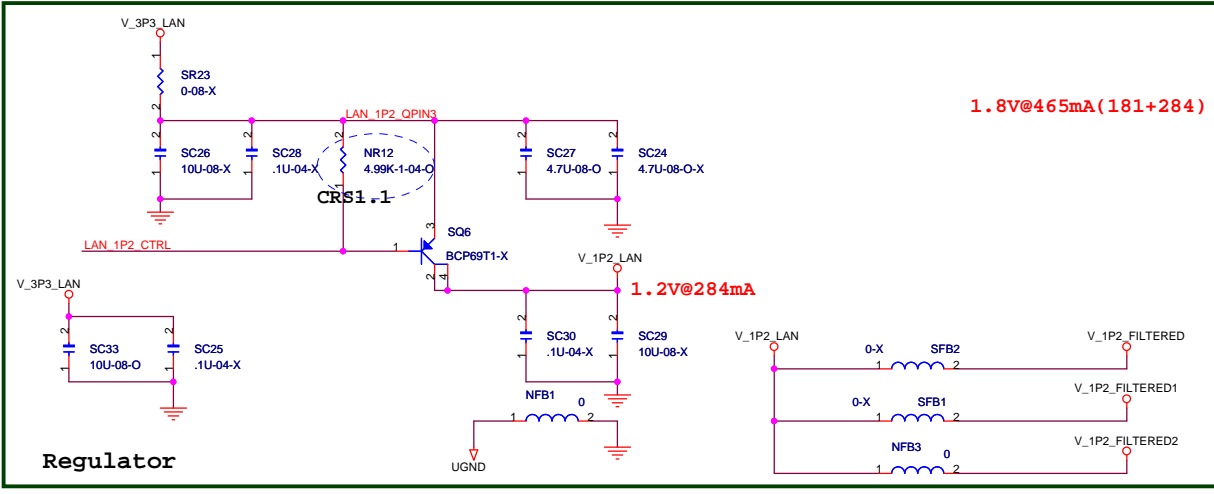
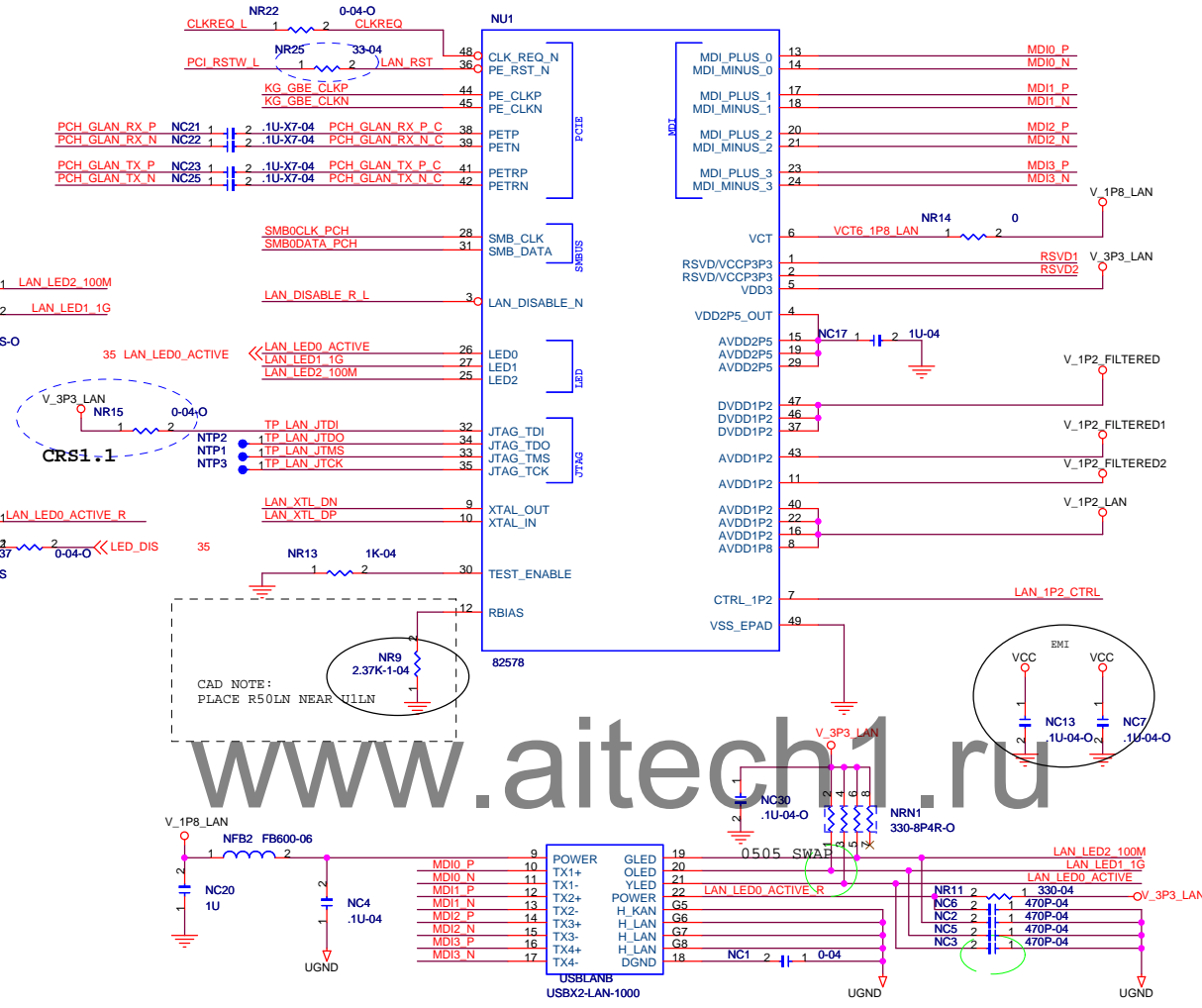
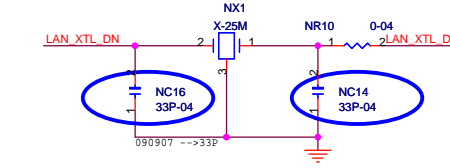
Input Equalization setting: Internal pull up ~150Kohm
A_EQ/B_EQ = LOW: For short and medium length PCB traces
A_EQ/B_EQ = HIGH: For long length PCB traces

Output Pre-emphasis Setting: Internal pull down ~150Kohm
A_PRE/B_PRE = LOW, Pre-emphasis disabled
A_PRE/B_PRE = HIGH, Pre-emphasis enabled



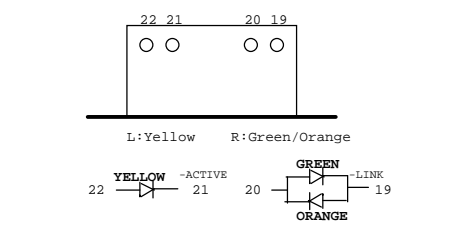
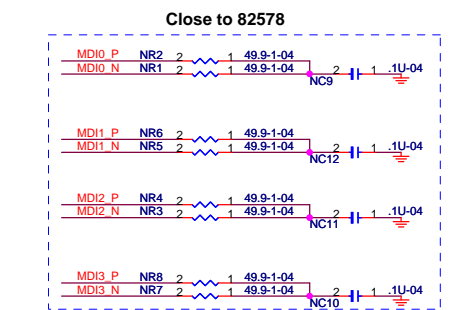
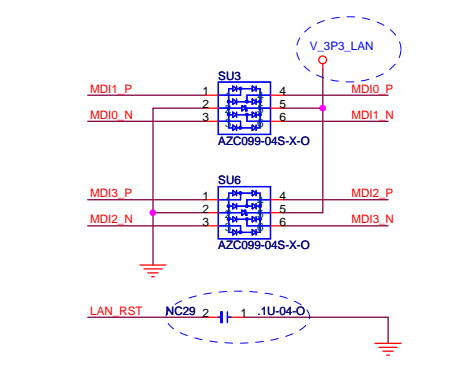


Crystal Spec: $\pm 30\text{ppm}$, $CL=20\text{pF}$
 $Ce=2*CL - (Cs+Ci)$

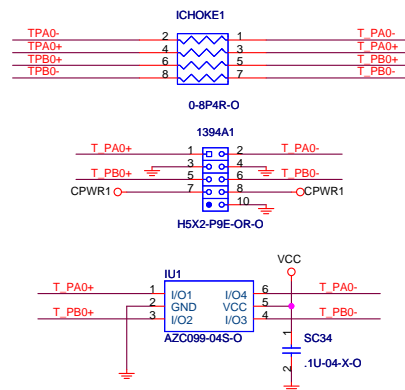
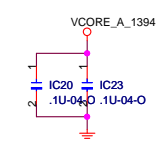
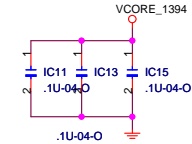
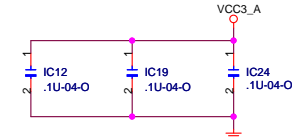
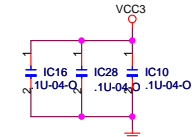
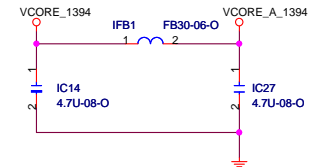
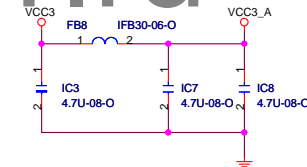
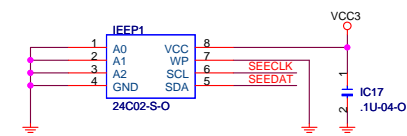
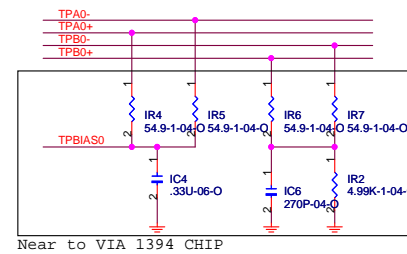
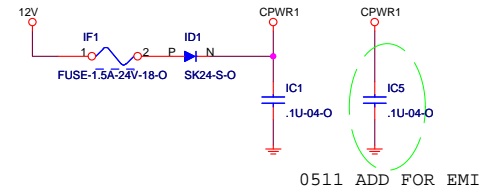


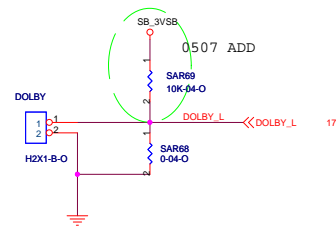
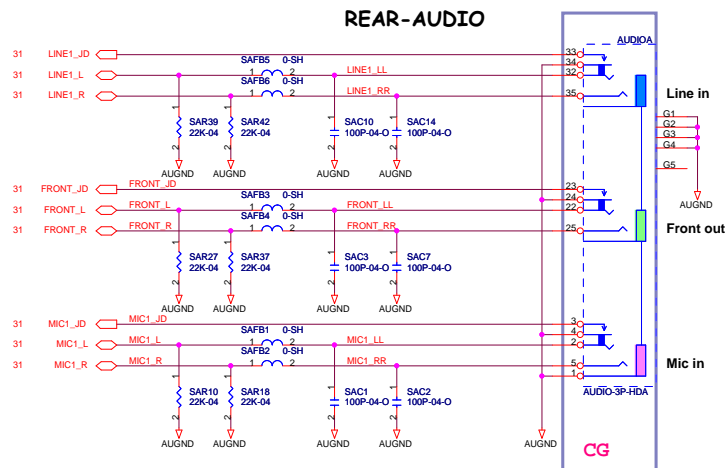
WOL	Status	Yellow	Gre/Ora
Don't Care	No link	OFF	OFF
OFF	S3/S4/S5	OFF	OFF
ON	10M,Inactive	OFF	OFF
ON	10M,Active	YB	OFF
ON	100M/Inactive	OFF	G
ON	100M/Active	YB	G
ON	1G,Inactive	OFF	O
ON	1G/Active	YB	O

Remark: Y/G/O-->Color, B-->Blinking

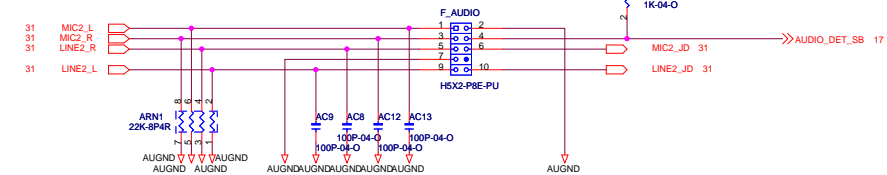


shadow EEPROM	ON	OFF
R215	V	X



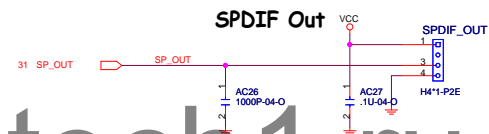


FRONT-AUDIO

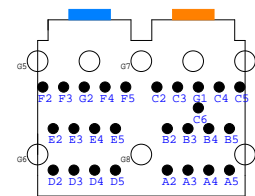
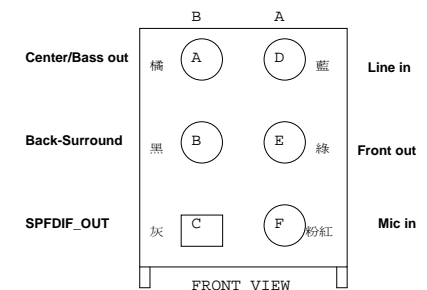
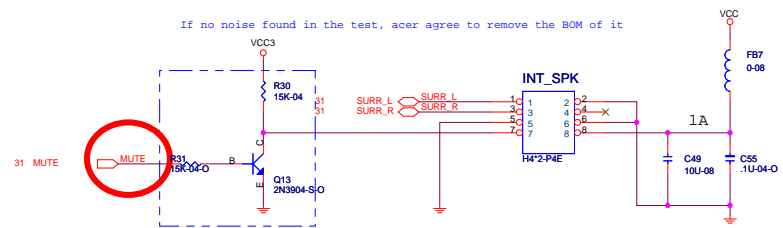


GPI: cable detection	
LOW	Plug cable
HIGH	No plug cable

SPDIF Out



If no noise found in the test, acer agree to remove the BOM of it



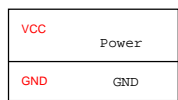


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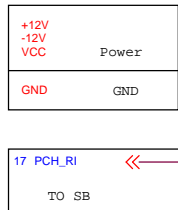
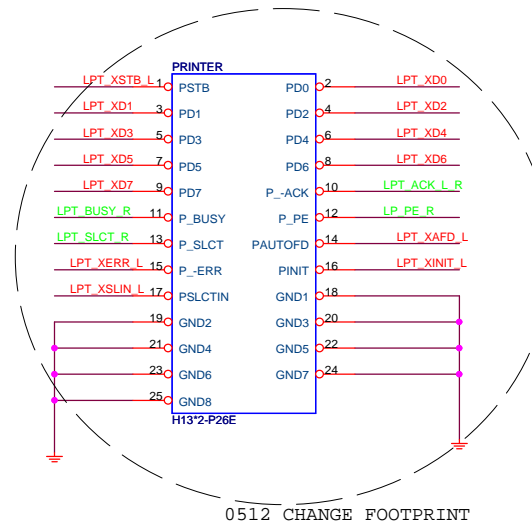
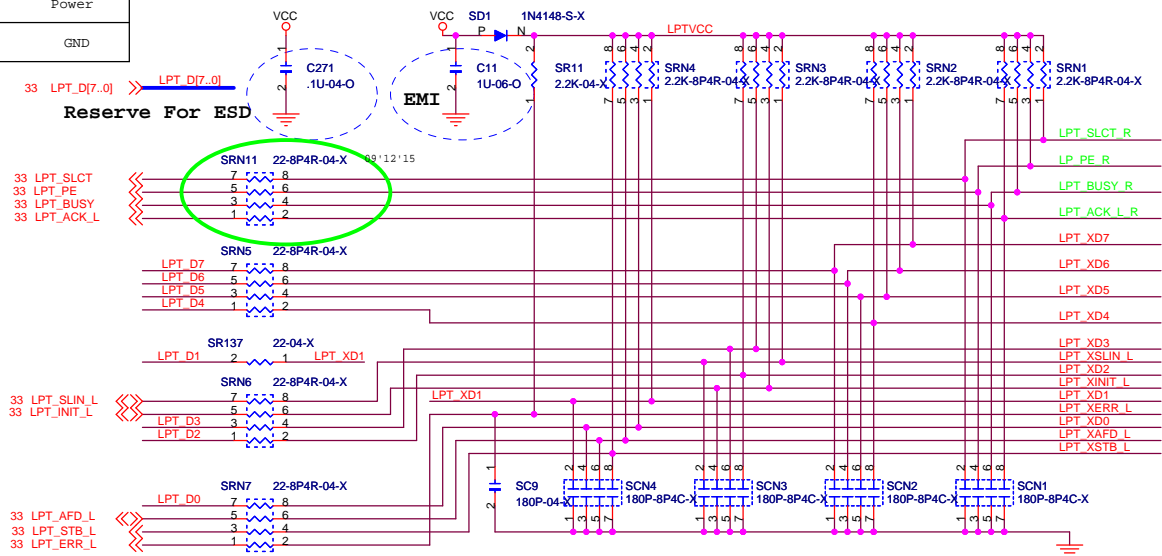
SIO IT8721F-BX

Document Number **H57H-AD** Rev 1.0

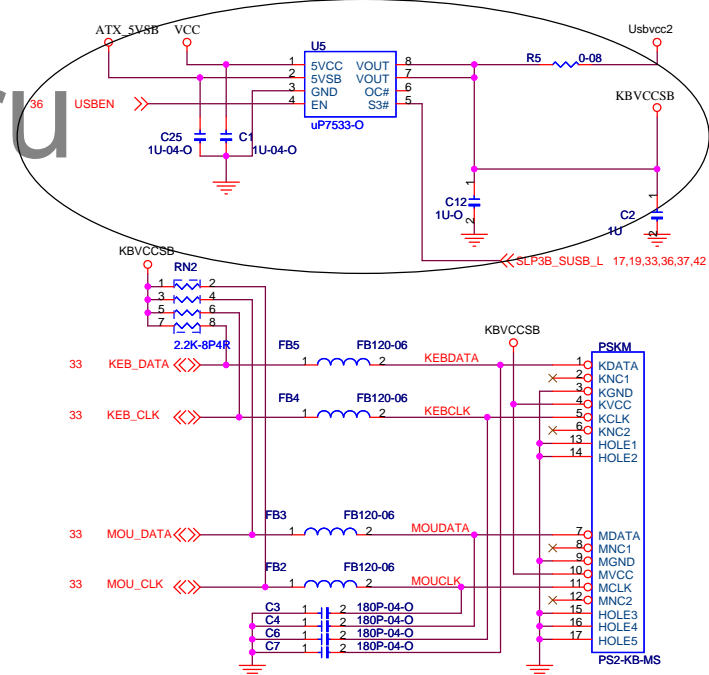
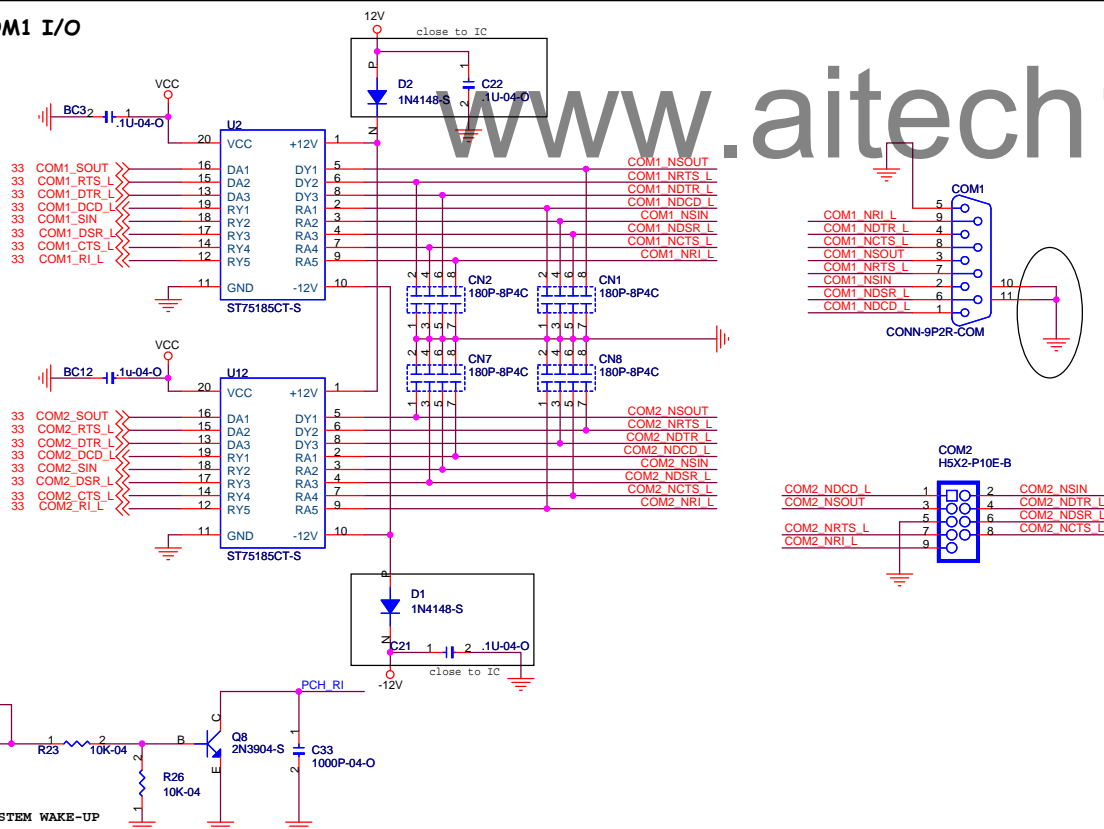
Date: Tuesday, January 19, 2010 Sheet 33 of 45



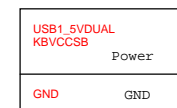
LPT



COM1 I/O



KEYBOARD & MOUSE

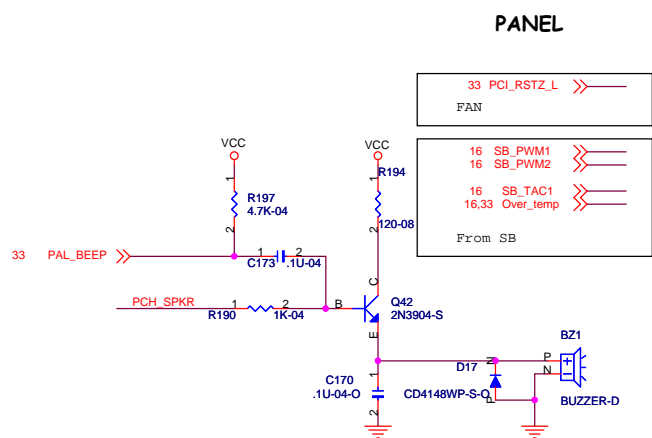


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Title: COM&PS2&FDD&LPT

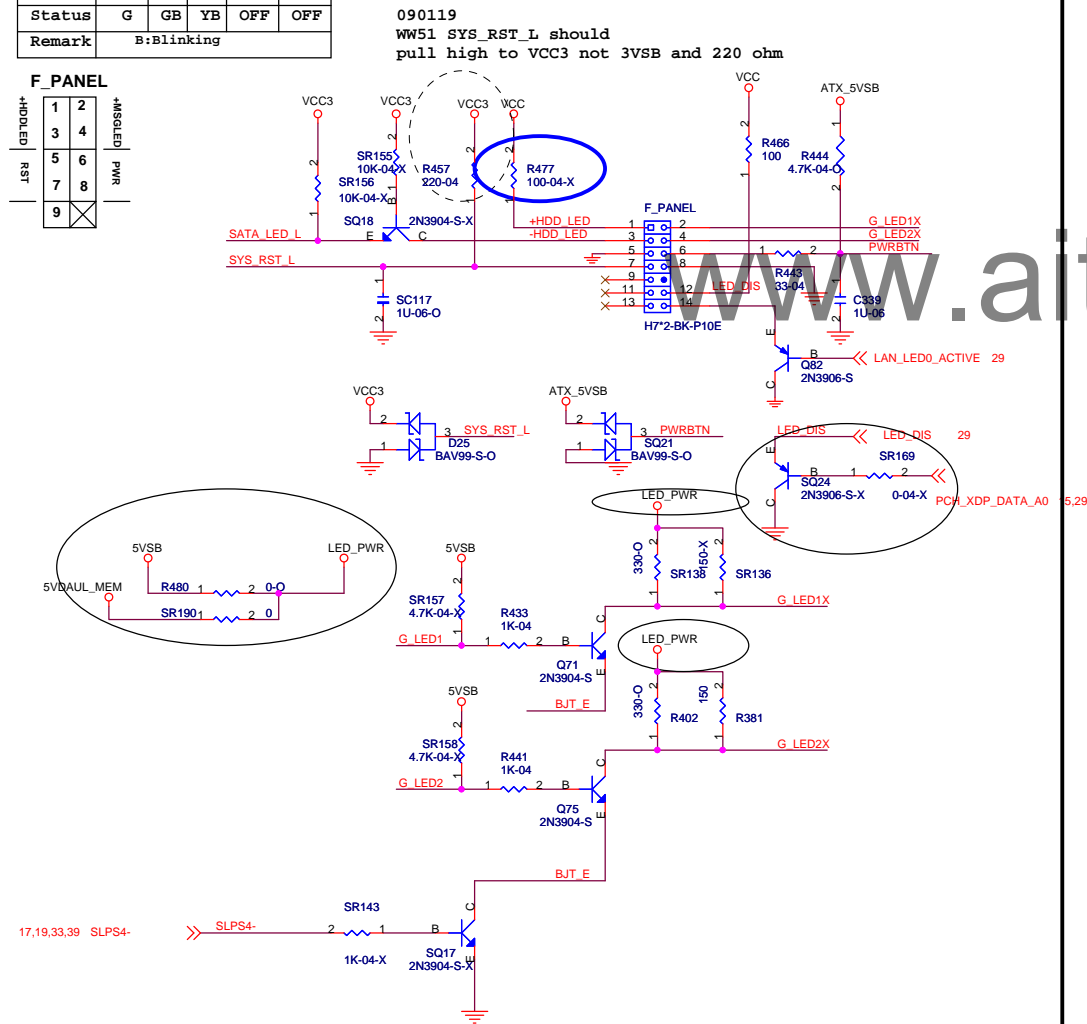
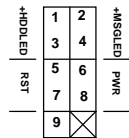
Size: Custom Document Number: H57H-AD Rev: 1.0

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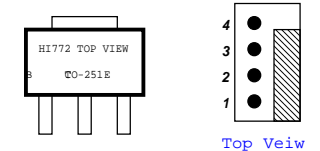
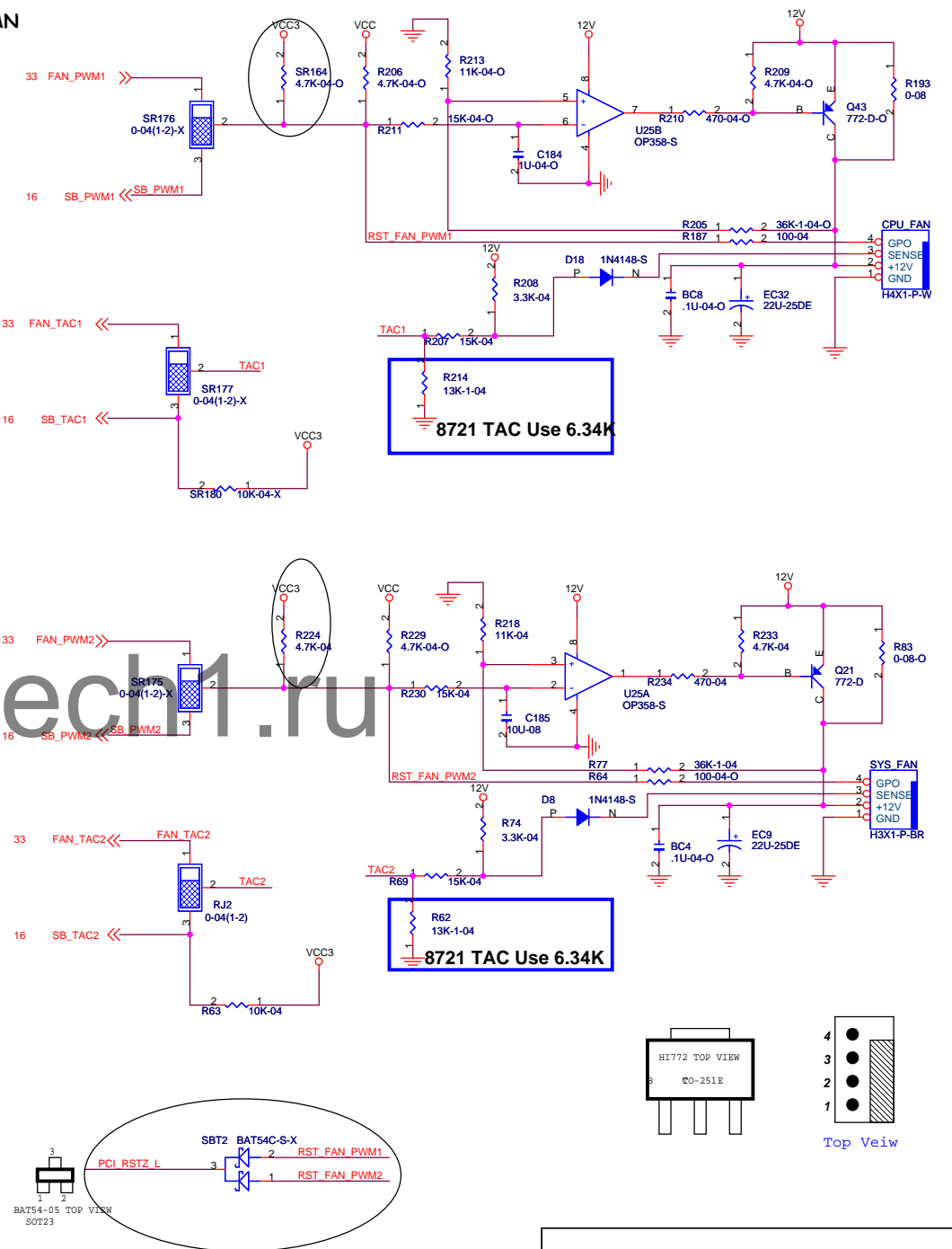


	S0	S1	S3	S4	S5
G_LED1	L	B	B	L	L
G_LED2	H	H	L	L	L
Status	G	GB	YB	OFF	OFF
Remark	B:Blinking				

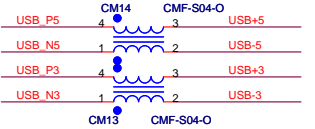
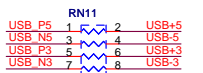
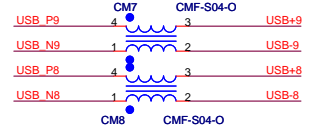
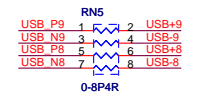
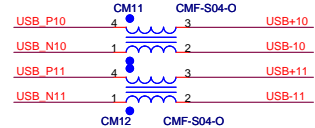
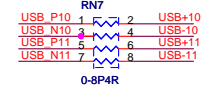
F_PANEL



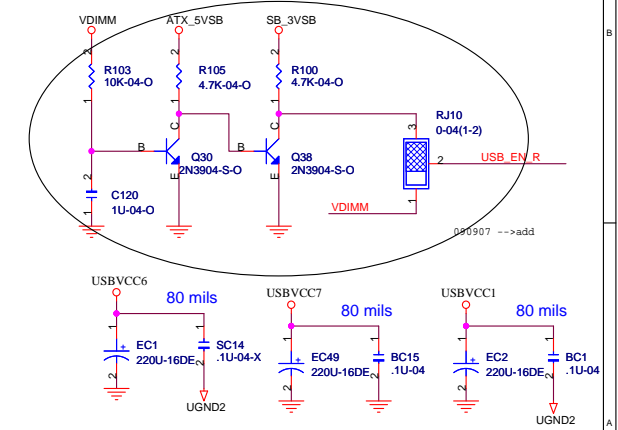
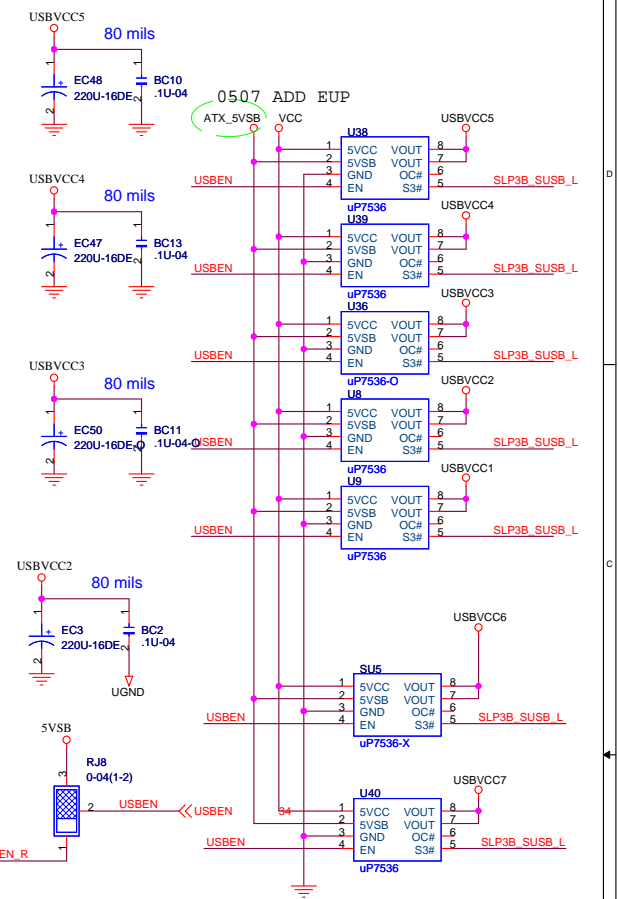
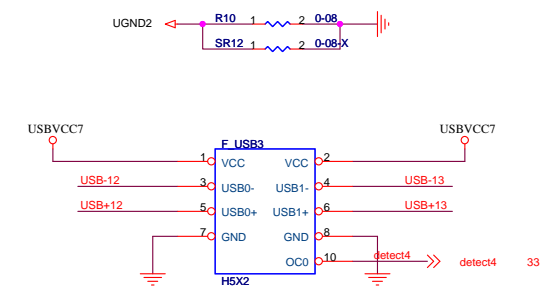
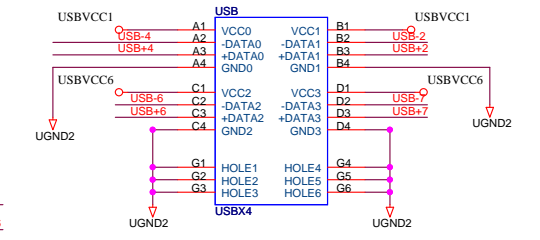
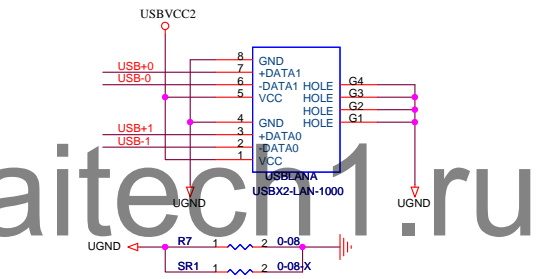
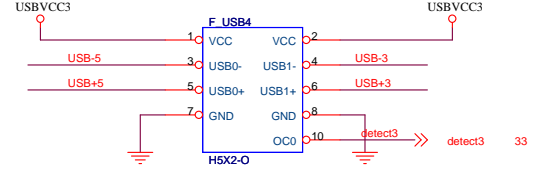
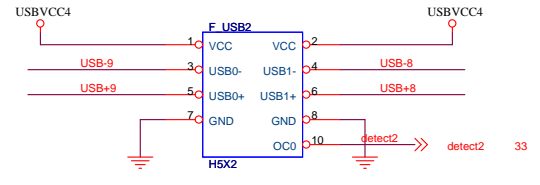
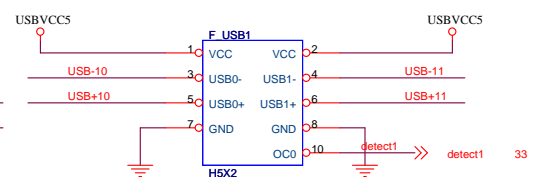
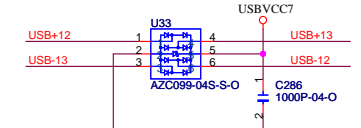
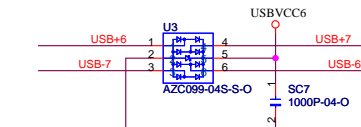
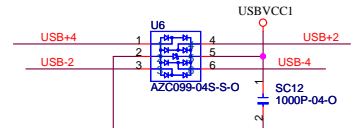
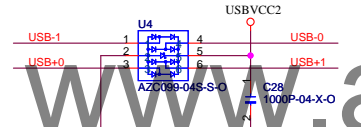
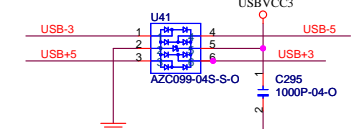
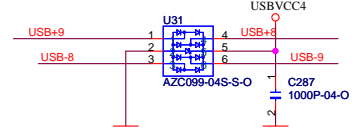
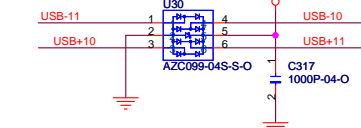
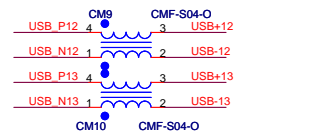
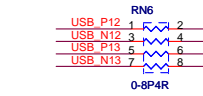
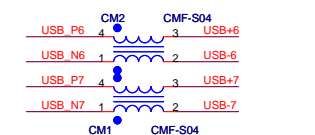
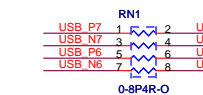
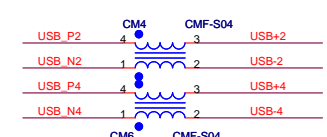
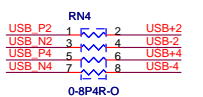
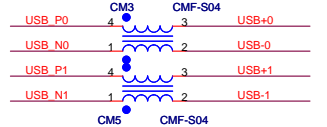
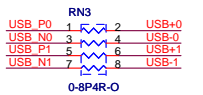
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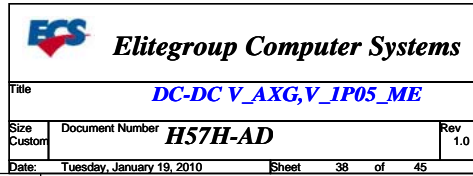


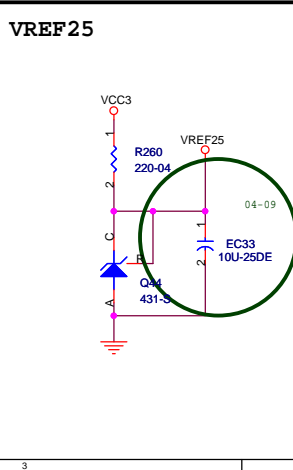
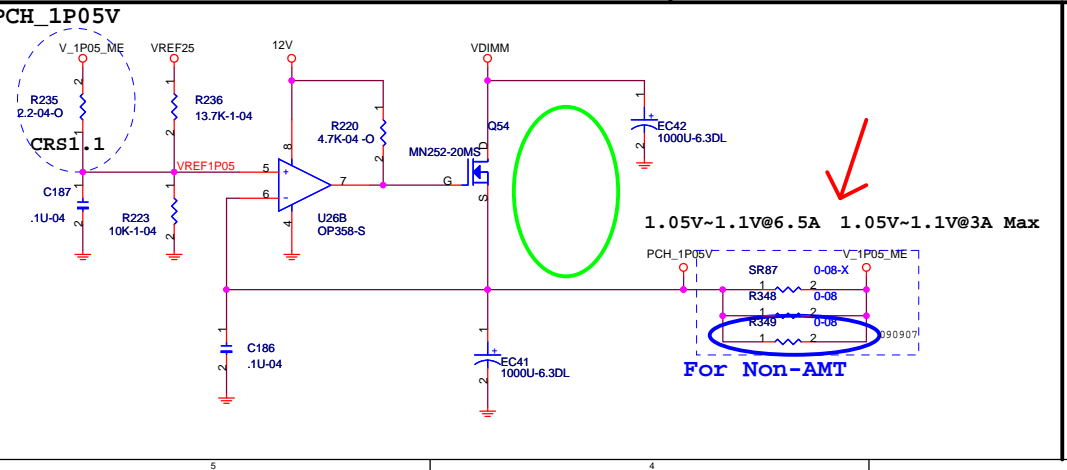
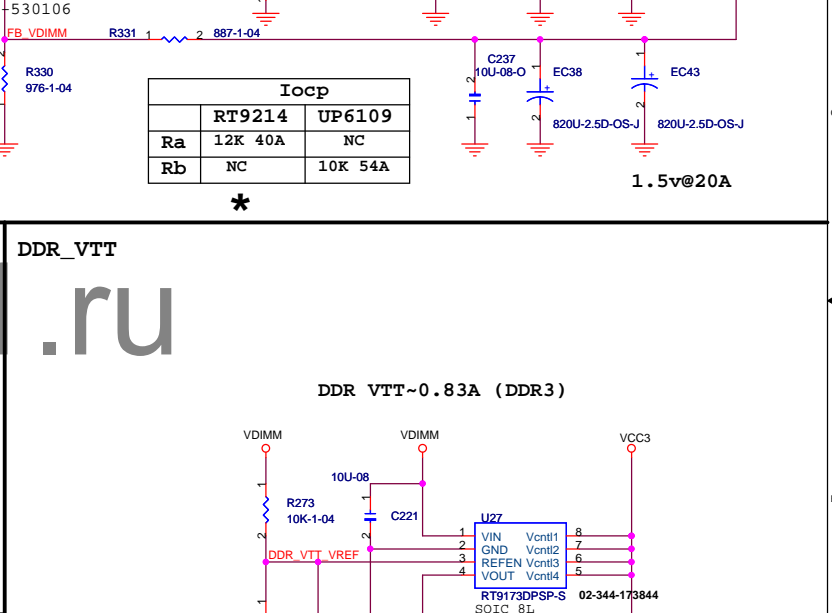
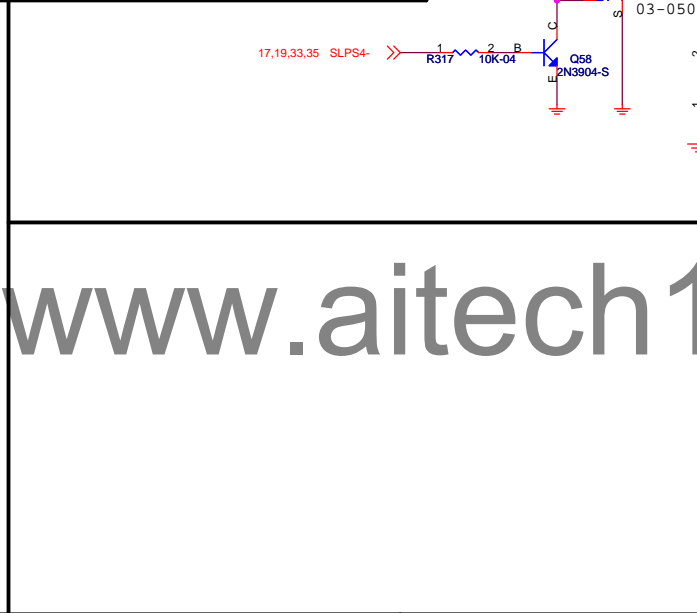
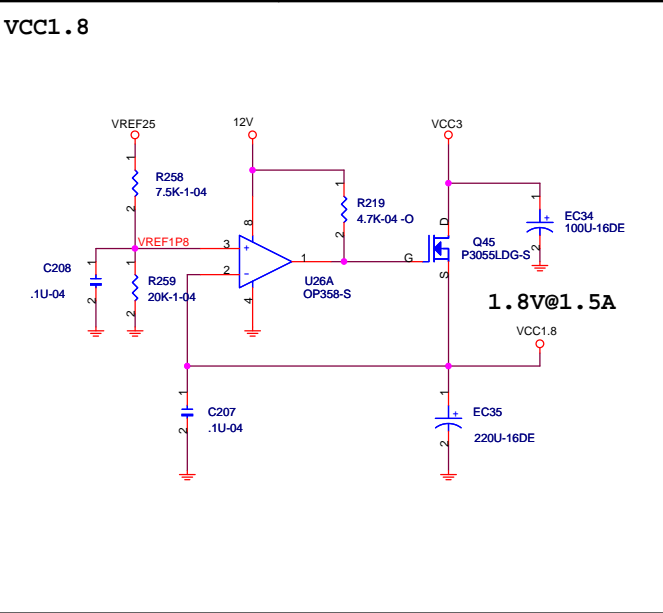
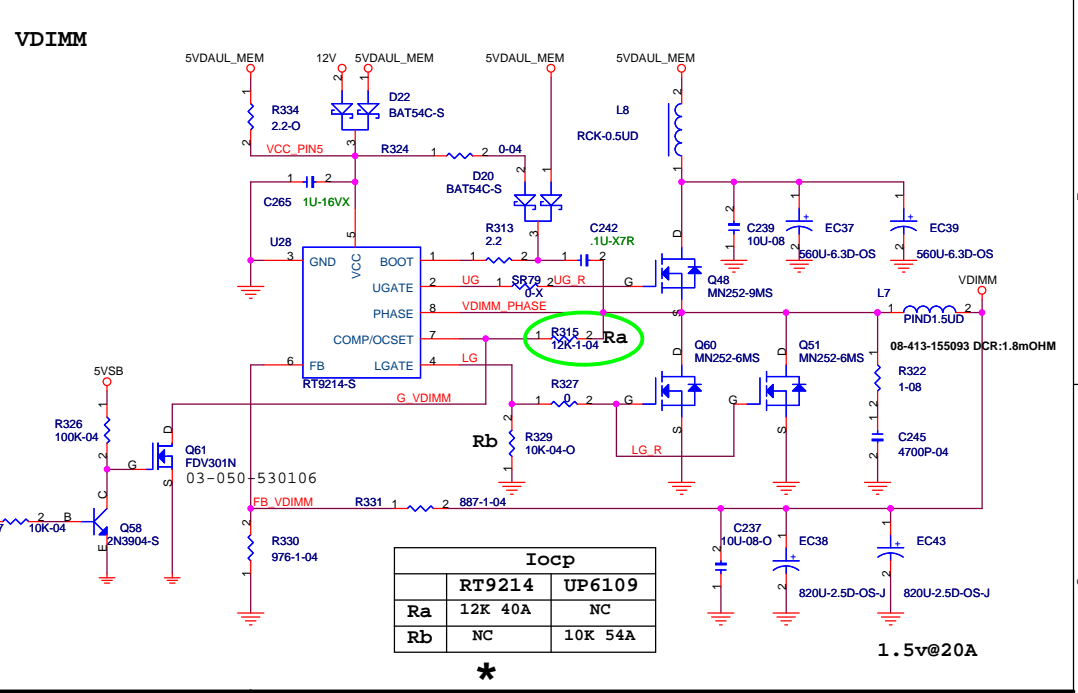
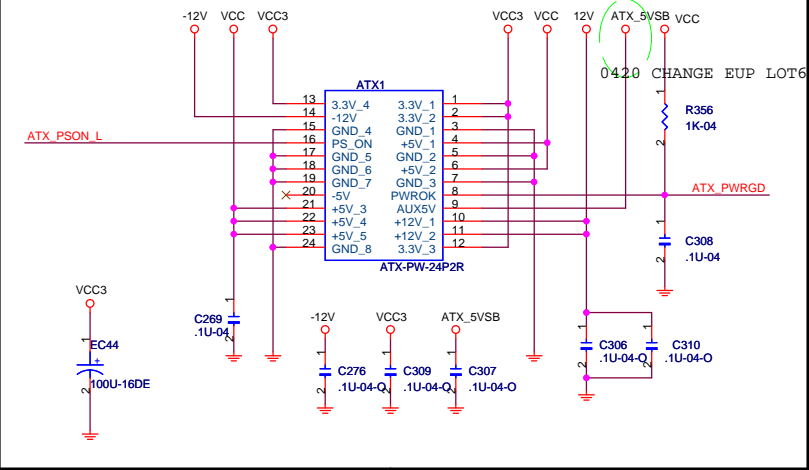
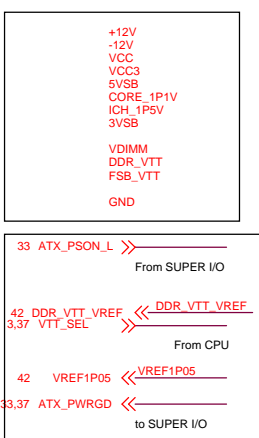
15 USB_P[13..0] >> USB_P[13..0]
 15 USB_N[13..0] >> USB_N[13..0]
 17,19,33,34,37,42 SLP3B_SUSB_L >> SLP3B_SUSB_L



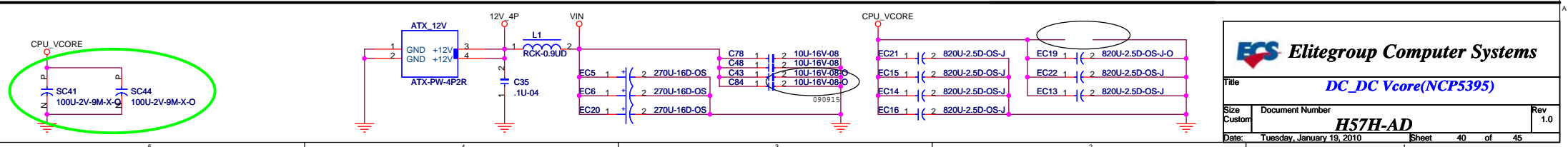
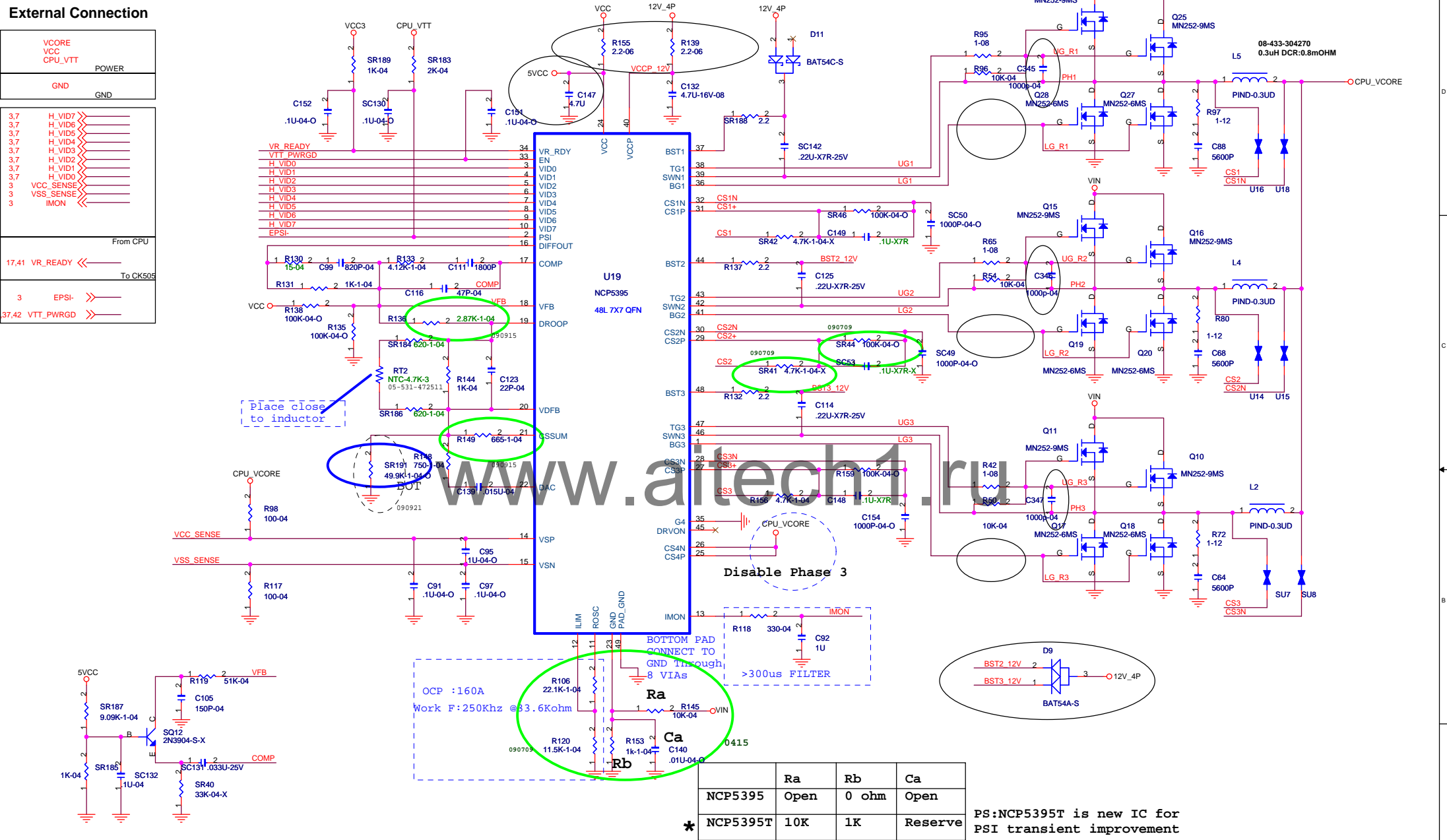
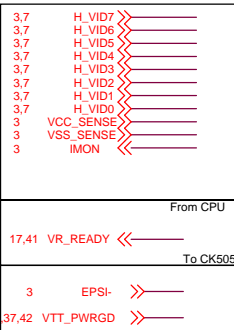
0429 CHANGE FOOTPRINT

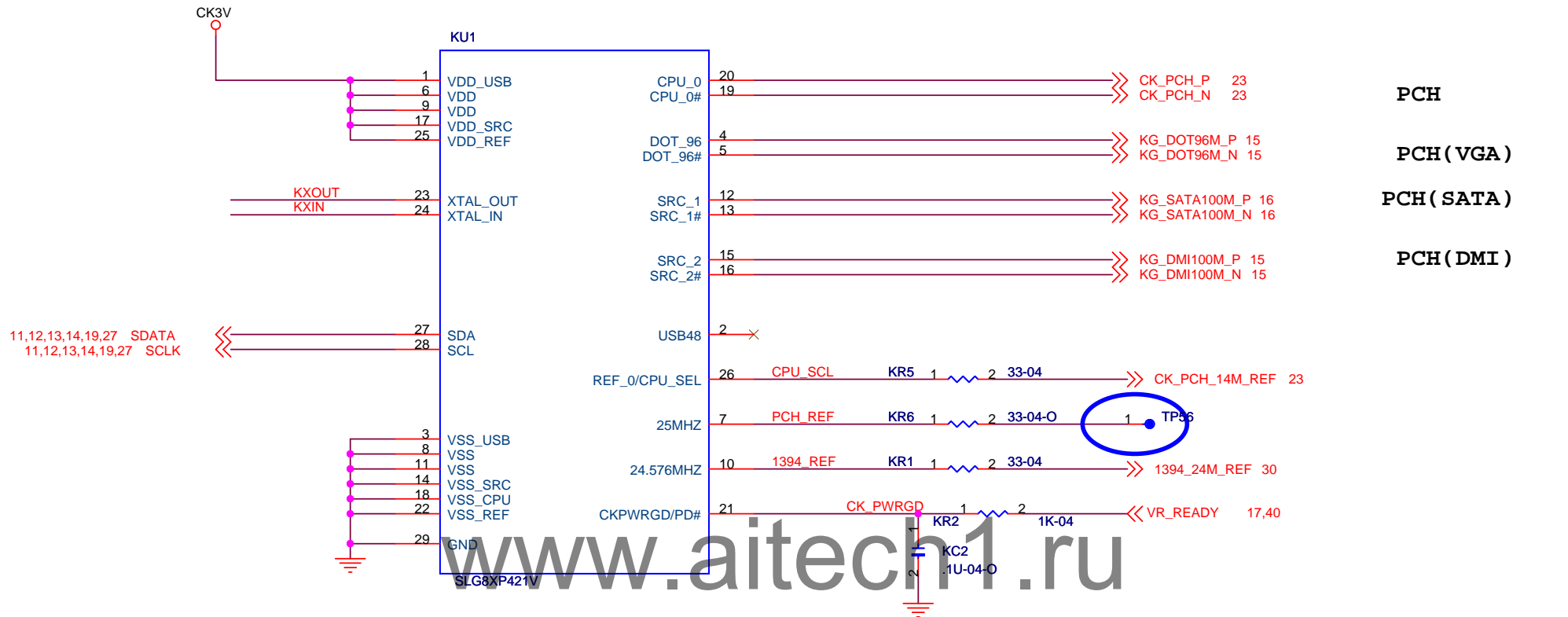




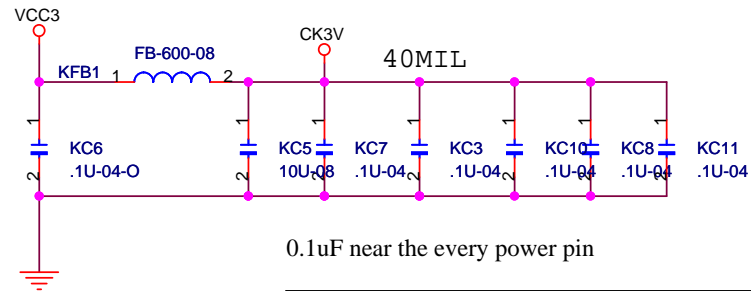
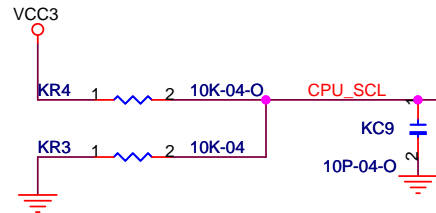
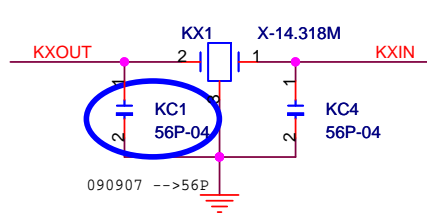


VCORE VCC CPU_VTT	POWER
GND	GND





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0.1uF near the every power pin

PIN 26	CPU_0
0 (default)	133MHz
1 (0.7-1.5V)	100MHz

Elitegroup Computer Systems

Title

SLG8XP421V

Size Custom

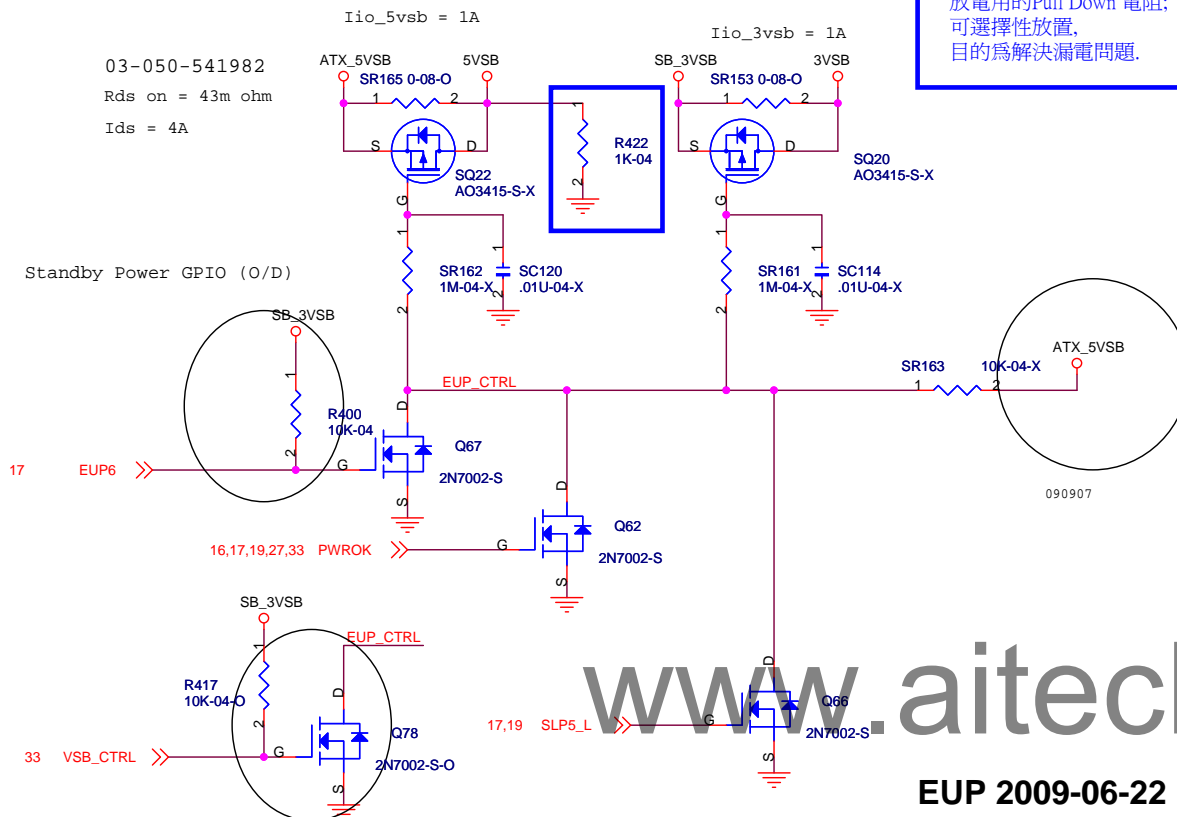
Document Number

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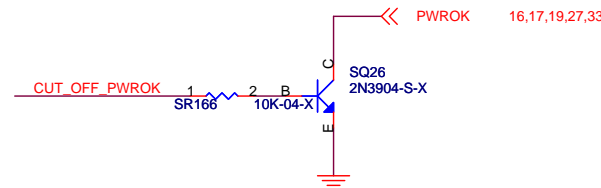
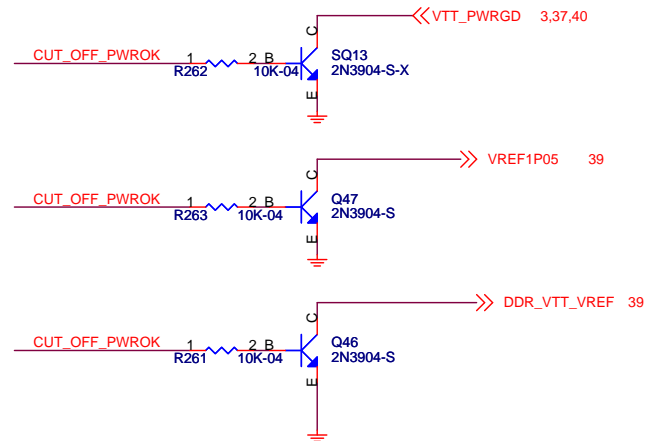
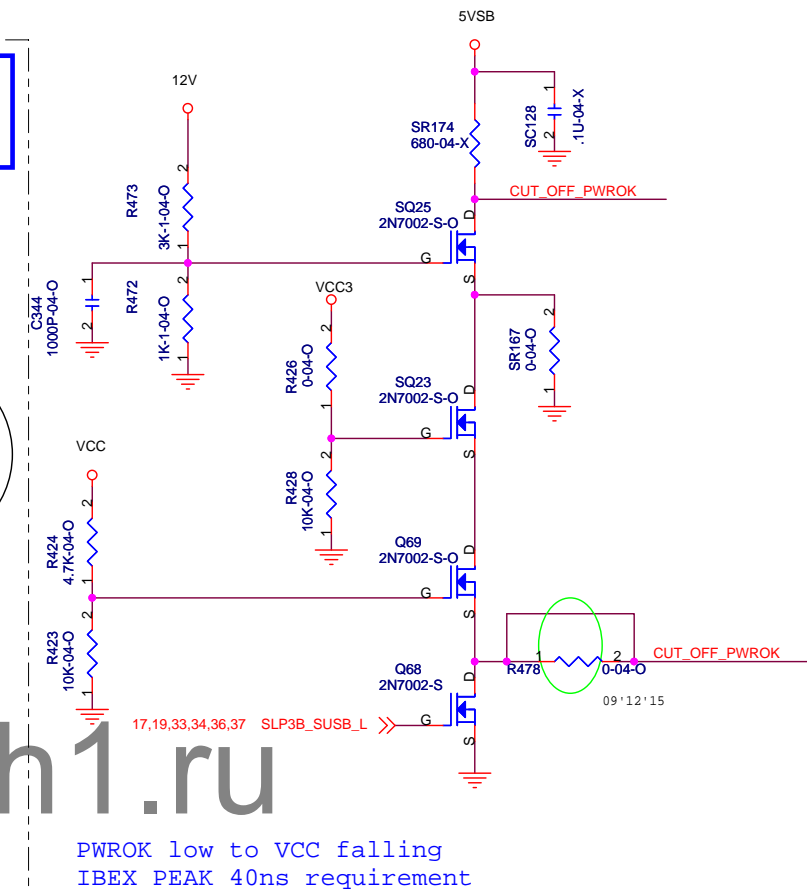
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Rev 1.0



放電用的Pull Down 電阻;
可選擇性放置,
目的為解決漏電問題.



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